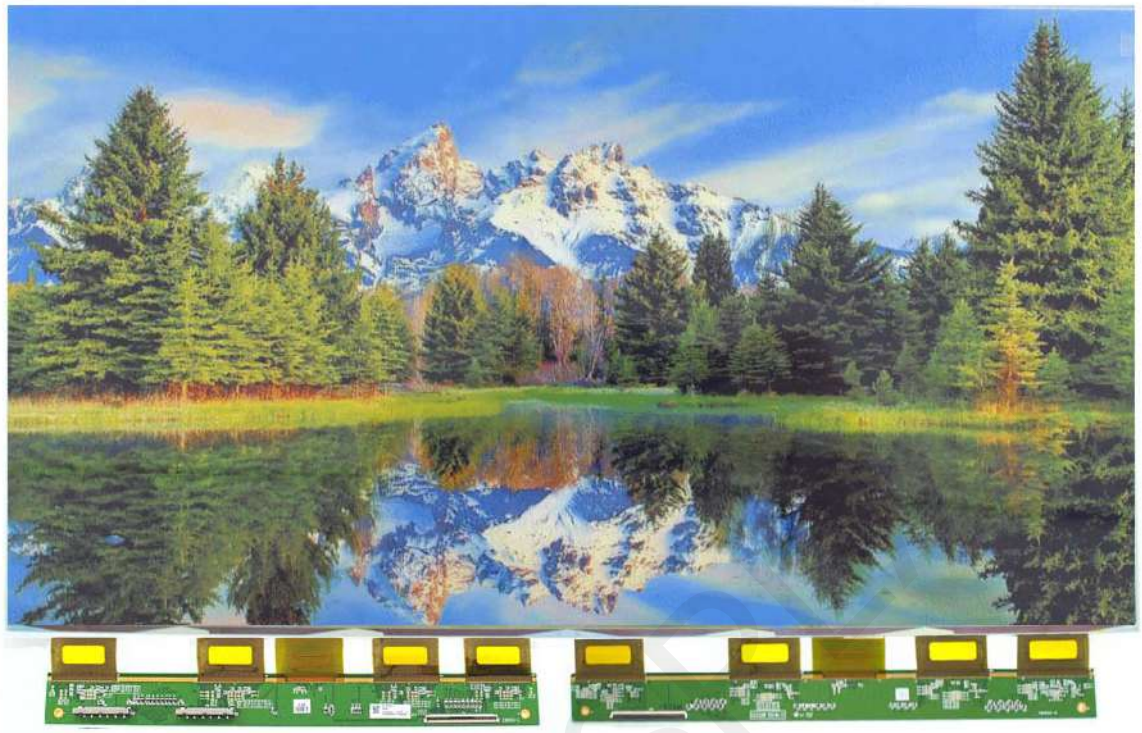
GooDisplay

31.5 inch
E-paper Display Series
GDEP315C01

Dalian Good Display Co., Ltd.

GooDisplay®

Product Specifications



Customer	**Standard**
Description	**31.5" E-PAPER DISPLAY**
Model Name	**GDEP315C01**
Date	**2024/06/04**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
	宝玉刘印	燕修印凤	之吴印良

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CONTENTS

1. General Description

GDEP315C01 is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 31.5” active area with 2560 x 1440 pixels and 16 : 9 aspect ratios. The display is capable to display images at red/green/blue/yellow/black/white depending on the display controller and the associated waveform file it used.

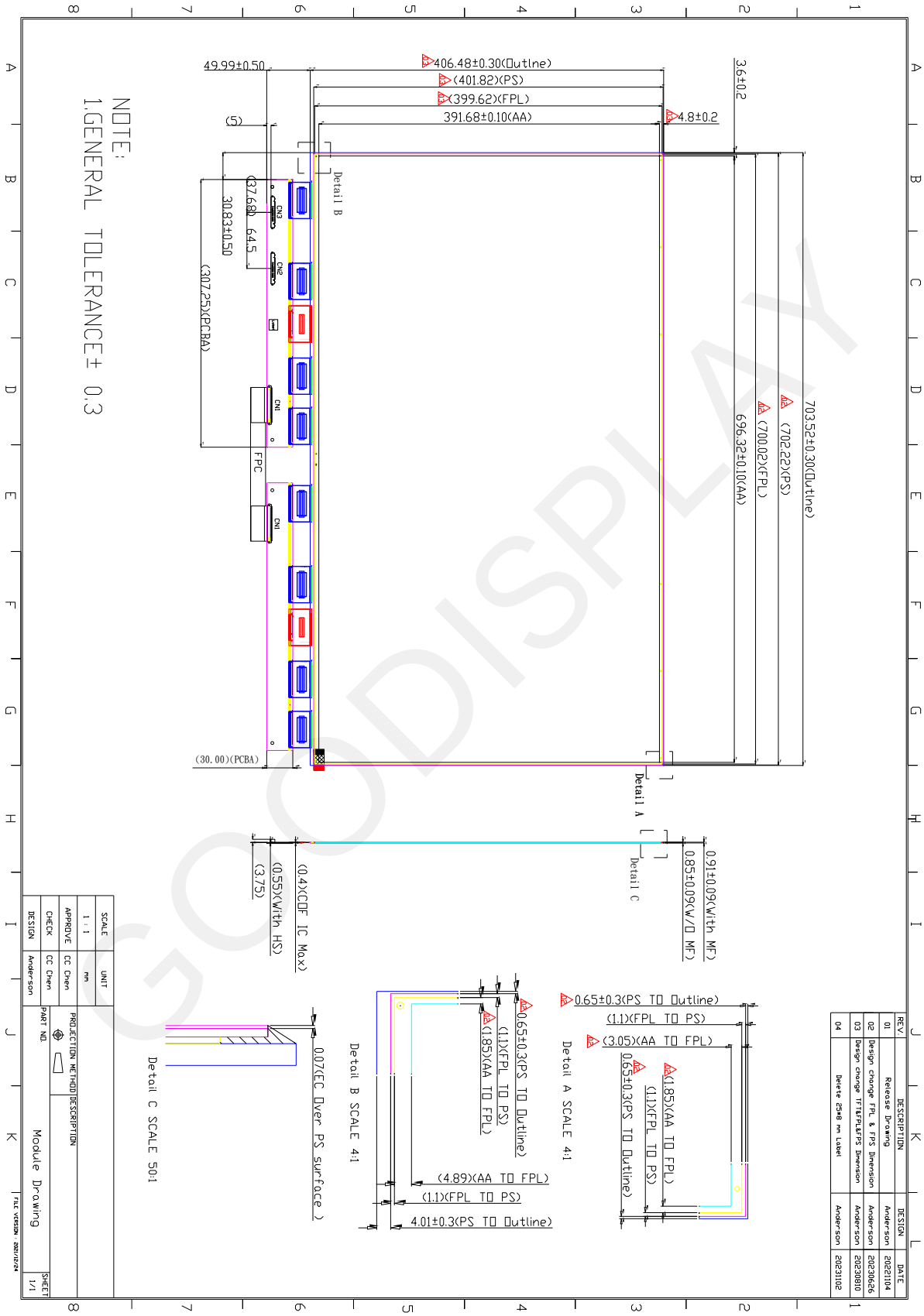
2. Features

- High contrast electrophoretic imaging film
- 2560 x 1440 display
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-stable
- Landscape, portrait mode
- Commercial temperature range: 0℃~50℃

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	31.5	inch	94ppi
Display Resolution	2560(H) x 1440(V)	Pixel	16 : 9
Active Area	696.32 (H) x 391.68 (V)		
Pixel Pitch	0.272 x 0.272	mm	
Pixel Configuration	Square		
Outline Dimension	703.52 (H) x 406.48 (V) x 0.85(D)	mm	Without masking film
Module Weight	582 ± 20	g	
Display operating mode	Reflective mode		
FPL	E Ink Spectra 6		
Surface treatment	Anti-glare treatment for protective sheet		

4. Mechanical Drawing of EPD Module



5. Input / Output Interface

5.1 Connector type:

P-TWO 187059-51221 compatible

5.2 Pin ssignment

1) PCB_L

CON

Pin	Signal	I/O	Description	Remark
1	VSPHI	P	Positive power supply source driver.	
2	VSPHI	P	Positive power supply source driver.	
3	VSPHI	P	Positive power supply source driver.	
4	VSPLI	P	Positive power supply source driver.	
5	VSPLI	P	Positive power supply source driver.	
6	VSPLI	P	Positive power supply source driver.	
7	VSPL2I	P	Positive power supply source driver.	
8	VSPL2I	P	Positive power supply source driver.	
9	VSPL2I	P	Positive power supply source driver.	
10	VSNHI	P	Negative power supply source driver.	
11	VSNHI	P	Negative power supply source driver.	
12	VSNHI	P	Negative power supply source driver.	
13	VSNLI	P	Negative power supply source driver.	
14	VSNLI	P	Negative power supply source driver.	
15	VSNLI	P	Negative power supply source driver.	
16	VSNL2I	P	Negative power supply source driver.	
17	VSNL2I	P	Negative power supply source driver.	
18	VSNL2I	P	Negative power supply source driver.	
19	VPP	P	OTP power supply source driver.	
20	VPP	P	OTP power supply source driver.	
21	GND	G	Ground	
22	GND	G	Ground	
23	VGH	P	Positive power supply gate driver.	
24	VGH	P	Positive power supply gate driver.	
25	AVDD	P	DCDC power input voltage	
26	AVDD	P	DCDC power input voltage	
27	AVDD	P	DCDC power input voltage	
28	VDD	P	Analog /digital voltage supply for source Driver IC.	
29	VDD	P	Analog /digital voltage supply for source Driver IC.	
30	VCC	P	Common Voltage for source Driver IC Oscillator.	
31	VCC	P	Common Voltage for source Driver IC Oscillator.	
32	VDDN	P	Negative power supply for analog circuit.	
33	VDDN	P	Negative power supply for analog circuit.	
34	VDDN	P	Negative power supply for analog circuit.	
35	VGL	P	Negative power supply gate driver.	
36	VGL	P	Negative power supply gate driver.	
37	VDDP	P	Positive power supply for analog circuit.	
38	VDDP	P	Positive power supply for analog circuit.	
39	VDDP	P	Positive power supply for analog circuit.	
40	Boder	P	Border output pin for check voltage	
41	Boder	P	Border output pin for check voltage	

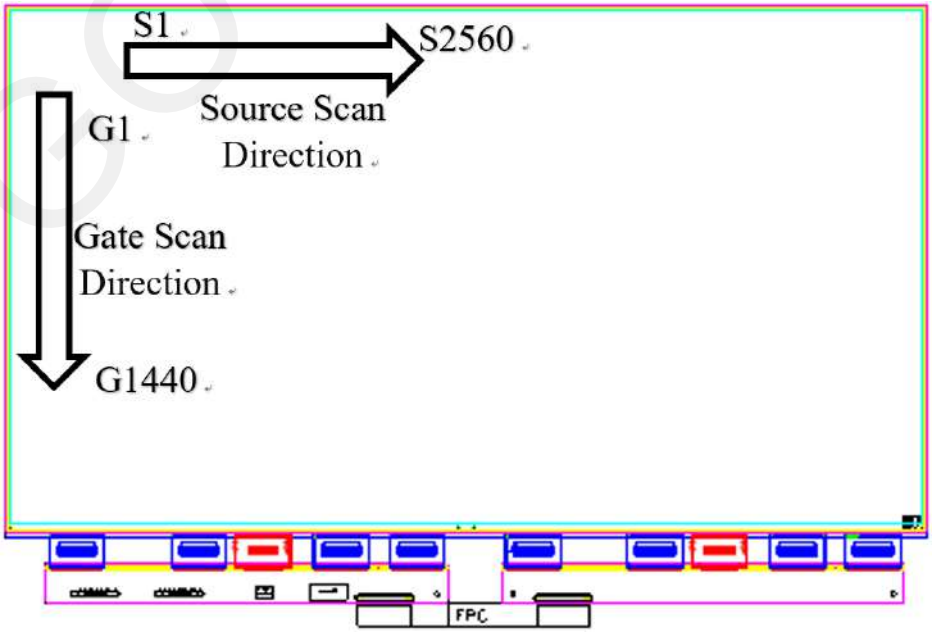
42	VCOMBD	P	Border Buffer output. Connect a 0.47uF stabilizing capacitor application circuit.	
43	VCOMBD	P	Border Buffer output. Connect a 0.47uF stabilizing capacitor application circuit.	
44	VNCP-3P5V	P	Negative power supply for analog circuit for TFT Vcom	
45	VNCP-3P5V	P	Negative power supply for analog circuit for TFT Vcom	
46	VBB-3P5V	P	Negative power supply for analog circuit for TFT Vcom	
47	VBB-3P5V	P	Negative power supply for analog circuit for TFT Vcom	
48	TFT-VCOM	P	Common Voltage	
49	TFT-VCOM	P	Common Voltage	
50	FPL-VCOM	P	Common Voltage	
51	FPL-VCOM	P	Common Voltage	

CON2

Pin	Signal	I/O	Description	Remark
1	R-CS0	IO	chip select for Serial data (right half)	
2	R-CS1	IO	chip select for Serial data (right half)	
3	R-CS2	IO	chip select for Serial data (right half)	
4	R-CS3	IO	chip select for Serial data (right half)	
5	R-SCL	IO	Serial communication clock input	
6	R-D_CX	IO	Command/Data input. L: command H: data. (4-wire SPI). Connect to GND in 3-wire mode or standard 4-wire mode.	
7	R-SI0	IO	SDA / MOSI of data signal source driver (Input/output of 3-wire/4-wire SPI) (input of Standard 4-wire SPI) (input of Standard 4-wire SPI quad mode)	
8	R-SI	IO	MISO of data signal source driver (output of Standard 4-wire SPI) (input of Standard 4-wire SPI quad mode)	
9	R-SI2	IO	Data signal source driver (input of Standard 4-wire SPI quad mode)	
10	R-SI3	IO	Data signal source driver (input of Standard 4-wire SPI quad mode)	
11	NC		No Connection	
12	NC		No Connection	
13	NC		No Connection	
14	NC		No Connection	
15	L-CS0	IO	chip select for Serial data (left half)	
16	L-CS1	IO	chip select for Serial data (left half)	
17	L-CS2	IO	chip select for Serial data (left half)	
18	L-CS3	IO	chip select for Serial data (left half)	
19	L-SCL	IO	Serial communication clock input	
20	L-D_CX	IO	Command/Data input. L: command H: data. (4-wire SPI). Connect to GND in 3-wire mode or standard 4-wire mode.	
21	L-SI0	IO	SDA / MOSI of data signal source driver (Input/output of 3-wire/4-wire SPI) (input of Standard 4-wire SPI) (input of Standard 4-wire SPI quad mode)	
22	L-SI1	IO	MISO of data signal source driver (output of Standard 4-wire SPI) (input of Standard 4-wire SPI quad mode)	
23	L-SI2	IO	Data signal source driver (input of Standard 4-wire SPI quad mode)	
24	L-SI3	IO	Data signal source driver (input of Standard 4-wire SPI quad mode)	

25	NC		No Connection	
26	NC		No Connection	
27	NC		No Connection	
28	RST_N	IO	Global reset pin. Low reset.	
29	BUSY_N	IO	This pin indicates the driver status of source driver. BUSY_N= ”0” : Driver is busy BUSY_N= ”1” : non-busy	
30	CL	IO	Clock input/output pin. Master: Clock output. Slave: Clock input.	
31	NC	-	No Connection	
32	NC		No Connection	
33	NC		No Connection	
34	NC		No Connection	
35	NC		No Connection	
36	NC		No Connection	
37	NC		No Connection	
38	NC		No Connection	
39	NC		No Connection	
40	NC		No Connection	
41	NC		No Connection	
42	NC		No Connection	
43	TSCL		I2C clock for external temperature sensor of source driver.	
44	TSDA		I2C data for external temperature sensor of source driver.	
45	NC		No Connection	
46	NC		No Connection	
47	NC		No Connection	
48	NC		No Connection	
49	NC		No Connection	
50	NC		No Connection	
51	NC		No Connection	

5.3 Panel Scan Directions



6. Electrical Characteristics

6.1 bsolute Maximum Rating:

Table 6-1 Absolution maxing rating: The conditions in the table should not be exceeded; otherwise, the panel may be damaged.

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +3.6	V	--
Logic Supply Voltage	VCC	-0.3 to 1.42	V	
Logic Supply Voltage	VNCP	0.3 to -4.2	V	
Logic Supply Voltage	VDDP	-0.5 to 21	V	
Logic Supply Voltage	VDDN	0.5 to -21	V	
Positive Supply Voltage	V_{POS}	-0.3 to +17	V	--
Negative Supply Voltage	V_{NEG}	0.3 to -17	V	--
Max .Drive Voltage Range	V_{POS} - V_{NEG}	-0.3 to 34	V	--
Supply Voltage	VGH	-0.3 to +30	V	--
Supply Voltage	VGL	0.3 to -25	V	--
Supply Range	VGH-VGL	0.3 to 55	V	--
Operating Temp. Range	TOTR	0 to 50	℃	--
Storage Temperature	TSTG	-25 to +50	℃	--

6.2 Panel DC Characteristics

Table 6-2 Panel DC characteristics: Please follow the table for the normal operation of the panel; otherwise, it may influence the panel's optical performance.
The standby power (PSTBY) is the consumed power when the panel controller is in standby mode. This value is only for reference since it depends on the performance of the panel controller (Whether there is wireless transmission function (WiFi & BLE) will seriously affect the power consumption.)

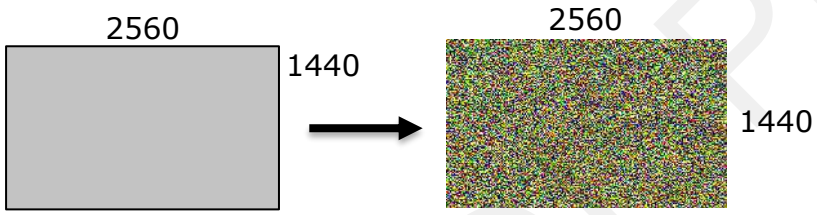
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V_{SS}		-	0	-	V
Logic Voltage supply	V_{DD}		2.7	3.3	3.6	V
	I_{VDD}	V_{DD}=3.3V		24.20	31.963	mA
Logic Voltage supply	VCC		1.3	1.35	1.4	V
	IVCC	V_{CC} =1.35		24.03	33.87	mA
Logic Voltage supply	VNCP		-3	-3.5	-4.5	V
	INCP	VNCP=-3.5		3.1	3.6	mA
Gate Negative supply	VGL		-21	-20	-19	V
	I_{VGL}	V_{GH} = -20V		42.09	61.098	mA
Gate Positive supply	VGH		26	27	28	V
	I_{VGH}	V_{GH} = +27V		3.43	4.798823	mA

Source Negative supply	V_{NEG1}		-16	-15	-14	V
	I_{NEG1}	V_{NEG1} = -15V	-	11.6	49.81941	mA
Source Negative supply	V_{NEG2}		TBD	Adjusted	TBD	V
	I_{NEG2}	V_{NEG2} = -9.8V	-	12.7	50.99538	mA
Source Negative supply	V_{NEG3}		TBD	Adjusted	TBD	V
	I_{NEG3}	V_{NEG3} = -9.1V	-	13.4	41.25576	mA
Source Positive supply	V_{POS1}		+14	+15	+16	V
	I_{POS1}	V_{POS1} = 15V		12.3	17.038	mA
Source Positive supply	V_{POS2}		TBD	Adjusted	TBD	V
	I_{POS2}	V_{POS2} = 9.2V		13.3	74.73576	mA
Source Positive supply	V_{POS3}		TBD	Adjusted	TBD	V
	I_{POS3}	V_{POS3} = 7.45V		12.4	17.03882	mA
Source Positive supply	V_{DDP}		+16	+19	+21	V
	I_{VDDP}	V_{DDP} =19V		1.06	28.596	mA
Source Positive supply	V_{DDN}		-21	-19	-16	V
	IV_{DDN}	V_{DDN} = -19V		11.6	13.97941	mA
Common voltage	V_{COM}			Adjusted		V
	I_{COM}	V_{COM} = -1.5V		11.03	14.53941	mA
Maximum power panel	Pmax				5038.623	mW
Typical power panel	Ptyp			2134.286		mW
Standby power panel	Pstby			1476		mW
Rush Current	IDD	VDD=3.3V			740	mA
	IVCC	V_{CC} =1.35			230	mA
	INCP	VNCP=-3.5			160	mA
	IGL	VGL=-20V			1100	mA
	IGH	VGH=27V			65	mA
	IN1	VN1=-15V			80	mA
	IN2	VN2=-9.8V			85	mA
	IN3	VN3=-9.1V			190	mA
	IP1	VP1=15V			70	mA
	IP2	VP2=9.2V			85	mA
	IP3	VP3=7.45V			260	mA

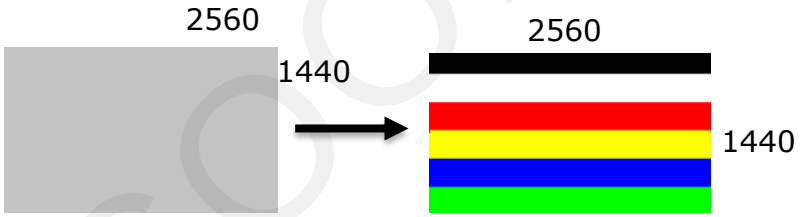
- The maximum power consumption is measured using 50Hz waveform with following pattern transition: Equivalent to each pixel of ink emerging from continuous white (Note 6-1)
- The Typical power consumption is measured using 50Hz waveform with following pattern transition: from continuous white scale pattern to basic colors bar. (Note 6-2)

- The standby power is the consumed power when the panel controller is in standby mode which here VDD, VCC, VDDN, VDDP, VNCP is ON while other power supplies are OFF.
- The listed electrical/optical characteristics are only guaranteed under the panel controller & waveform provided by E Ink.
- Vcom is recommended to be set in the range of assigned value ±0.2V.
- The rush current is for reference only since it depends on the driving capacity of the panel controller.
- Standby power panel is it depends on the panel controller (EVK) input power.

Note 6-1
The maximum power consumption



Note 6-2
The Typical power consumption



6.3 Refresh Rate

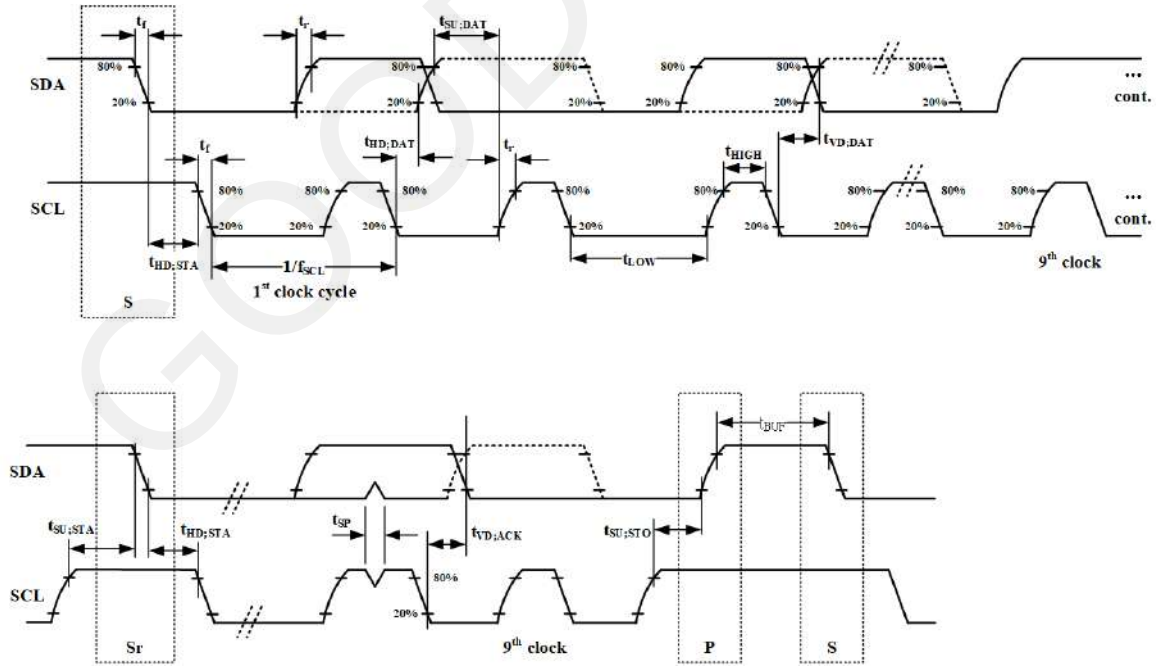
The module Polaris is applied at a maximum screen refresh rate of 50Hz.

	Min	Max
Refresh Rate	-	50HZ

6.4 Panel AC Characteristics

VDD=2.7V to 3.6V, unless otherwise specified. The timing parameter for each sub panel

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	FSCL	0		400	kHz
LOW period of the SCL clock	tLOW	0.6			us
HIGH period of the SCL clock	tHIGH	0.6			us
Rise time of both SDA and SCL signals	tr			300	ns
Fall time of both SDA and SCL signals	tf			300	ns
Bus free time between a STOP and START condition	tBUF	0.5			ns
Capacitive load for eachbus line	Cb			50	ns
Data valid time	tVD;DAT			0.45	ns
Data valid acknowledge time	tVD;ACK			0.45	ns
Setup time	TSU;STA TSU;STO	0.26			ns
	TSU;DAT	50			
Hold time	THD;STA	0.26			ns
	THD;DAT	0			



6.5 Controllers Timing (TBD)

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE)(3) and Gate Driver Clock (GDCK)(3). Note, that in this mode LGON follows GDCK timing.

6.6 Timing Parameters Table (TBD)

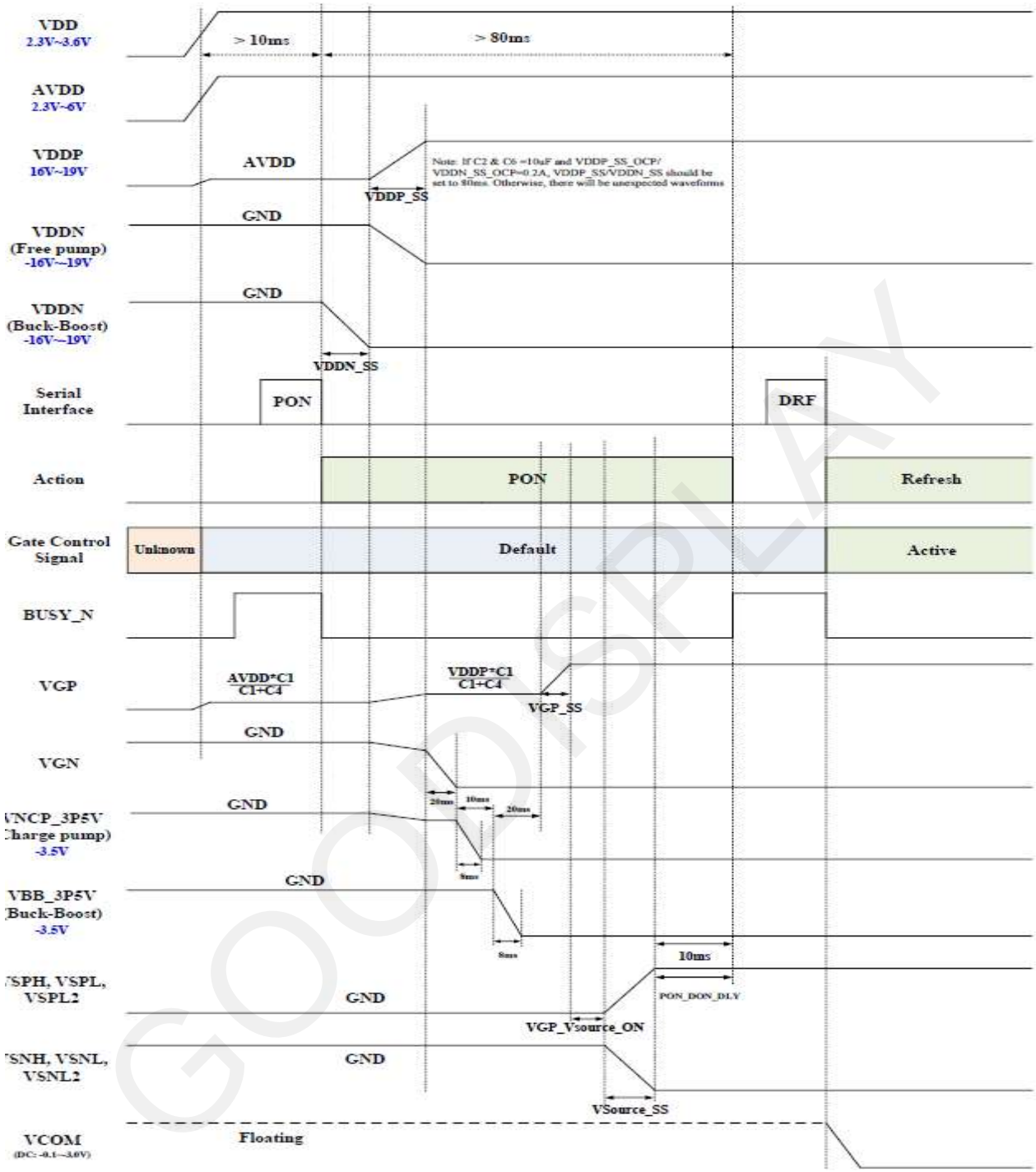
Timing Parameters Table (For 1 panel)

Mode	**3**	**Image Timing Resolution :** **5120 * 720**				
SDCLK[MHz]	**10**					
Pixels per SDCLK	**6**					
Line Parameters [SDCLK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
	22	**16**	**1280**	**42**	**28**	**600**
Line Parameters [us]						
Frame Parameters [Lines]	FSL	FBL	FDL	FEL	-	FR[Hz]
	1	**4**	**720**	**5**		**50**
Frame Parameters[us]						

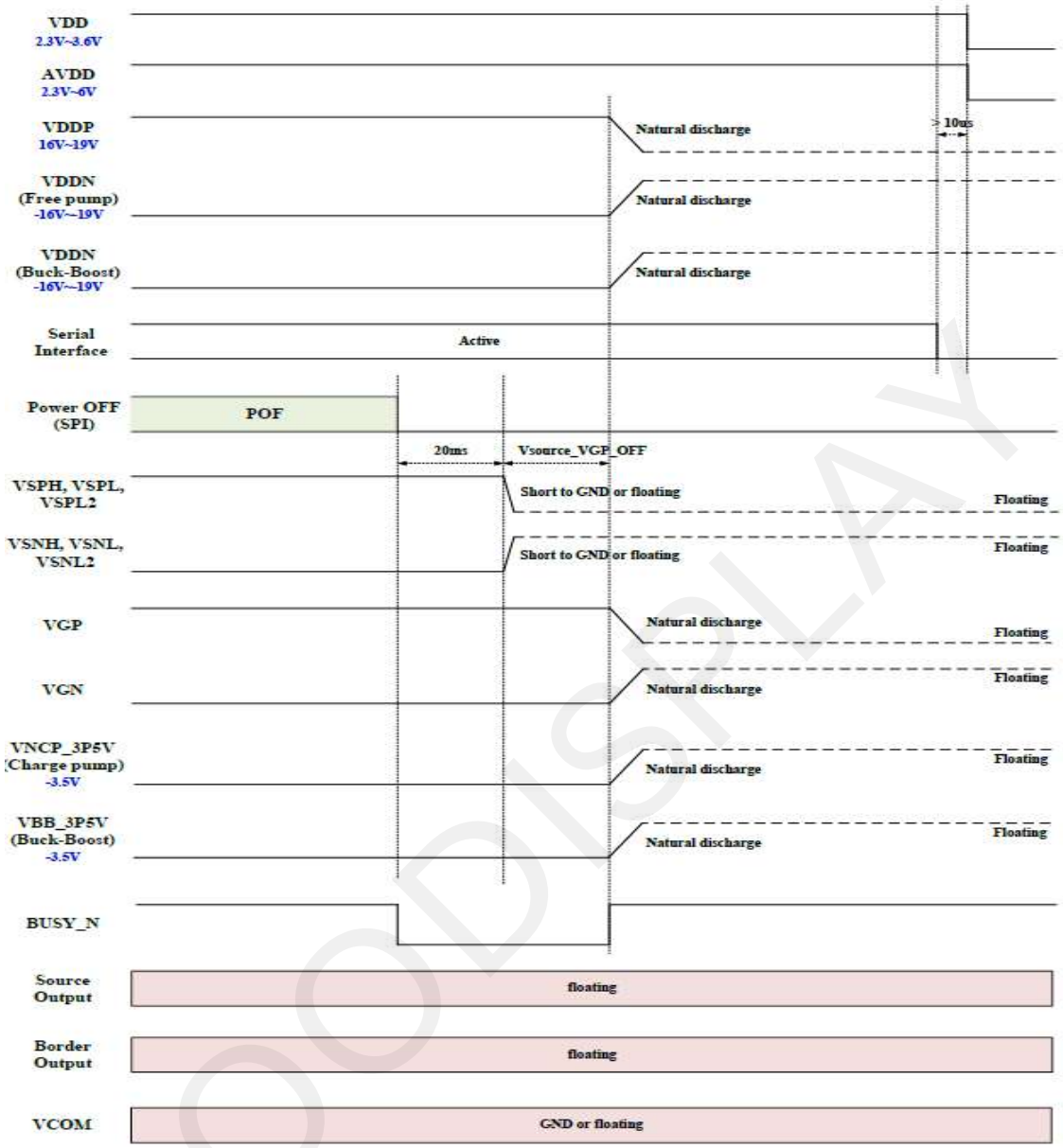
Note 1: For parameters definition, see Section 7. Active Matrix Electronic Paper Display Timings.

Note 2: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL

7. Power on Sequence



	Min	Max
TVDDS	10ms	-
TVDDPS	20ms	-
TVDDNS	20ms	-
TVGP_SS	20ms	-
TVGN_SS	20ms	-
TVNCP	10ms	-
TVOPS	10ms	-
TVNEG	10ms	-



	Min	Max	Remark
TVDDS	10μs	-	-
TVDDPS	20ms	-	-
TVDDNS	20ms	-	-
TVOPS	20ms	-	-
TVNEG	20ms	-	-

8. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

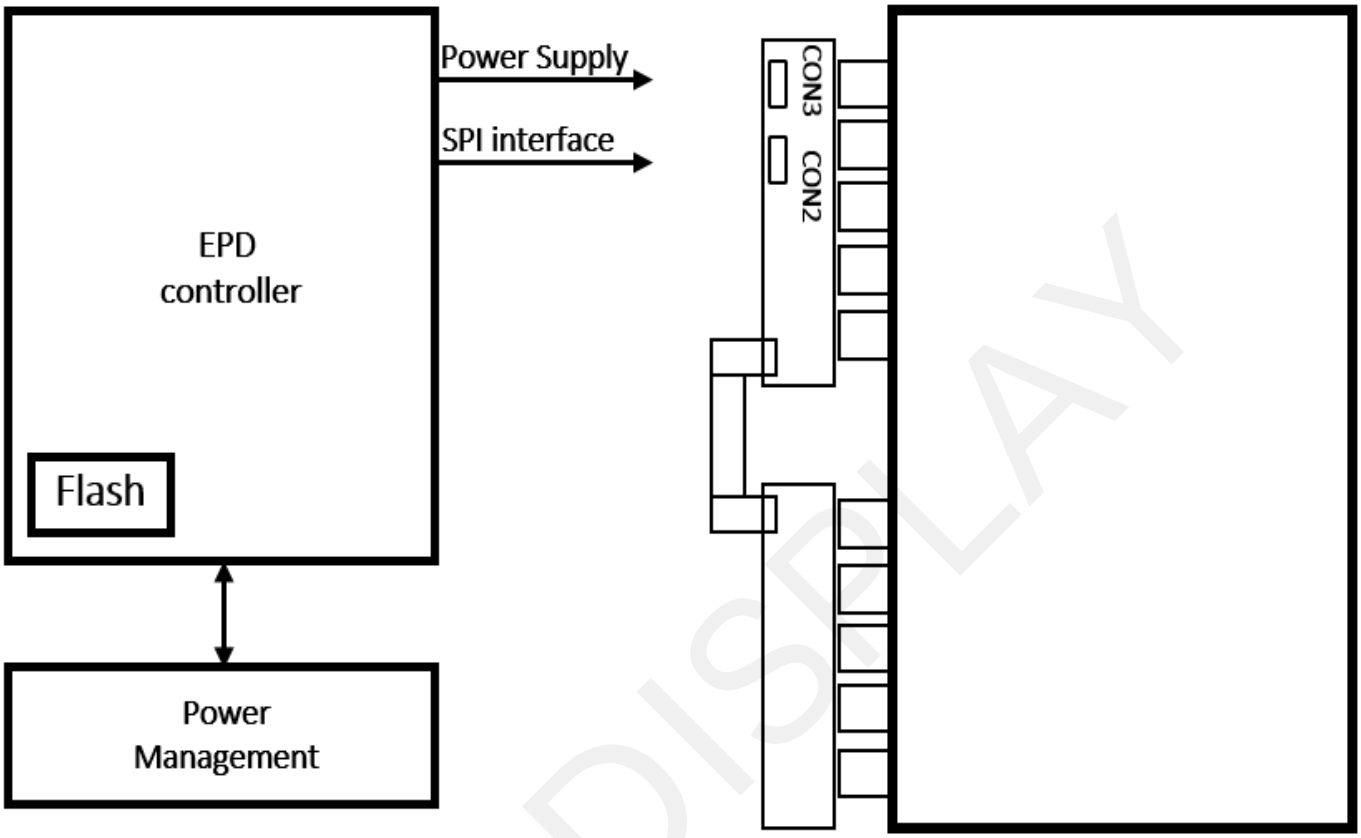
Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

9. Reliability Test (TBD)

#	RA item	Condition	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% , for 240 hrs	
2	Low-Temperature Operation	T = 0°C , for 240 hrs	
3	High-Temperature Storage	T = +60°C, RH=35% , for 240 hrs	
4	Low-Temperature Storage	T = -25°C , for 240 hrs	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% , for 240 hrs	
6	High Temperature, High-Humidity Storage	T = +60℃, RH=80% , for 240 hrs	
7	Temperature Cycle	-25℃ (30min) → +60℃ (30min), 50 Cycles	
8	Electrostatic Effect (non-operating)	(Machine model)+/- 250V, 0Ω, 200pF	
9	Package Vibration	Random wave(1.5Gms 10~200Hz) Direction: X,Y,Z 30mins per axes	
10	Package Drop Impact	Height :33cm 1 Corner , 3 Edges & 6 Faces	ASTM D 4169&5276 Level 2

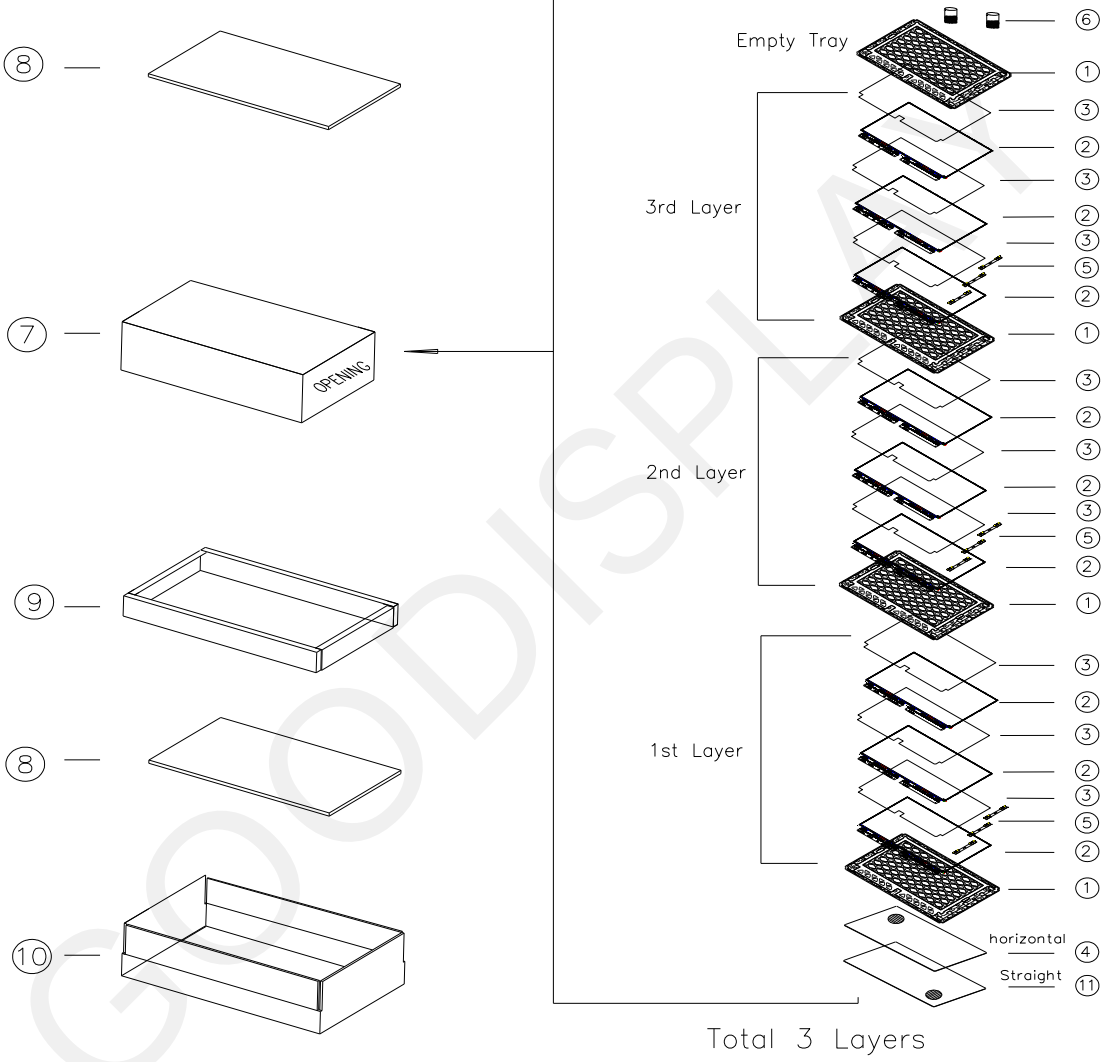
10. Block Diagram



11. Packing

11.1 Packing Drawing

REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	Anderson	20230302
02	Add Straight PP board	Anderson	20230818



NOTE:

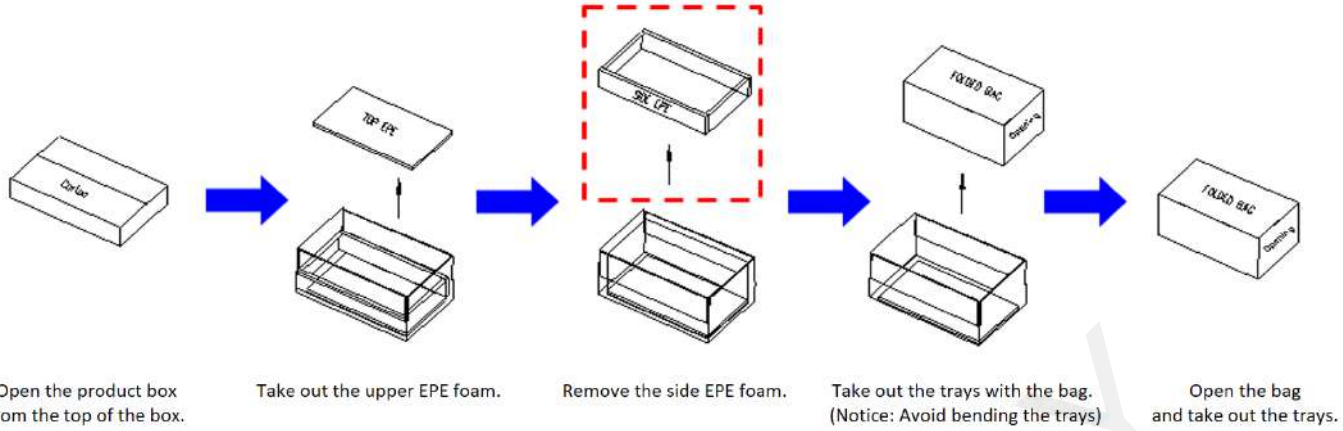
1. One layer include:
   3 pcs module /1 piece of tray
2. Q'TY: 9 pcs panel/carton
3. Dimension: 980*590*230mm

ITEM	DESCRIPTION	Q'TY	REMARK
11	PP BOARD	1	Straight
10	CARTON	1	
9	SIDE EPE	1	
8	U_D EPE	2	
7	FOLDED BAG	1	ANTISTATIC
6	30g DESICCANT	2	
5	FPC	9	
4	PP BOARD	1	Horizontal
3	EPE	9	ANTISTATIC
2	EPD	9	
1	TRAY	4	ANTISTATIC

APPROVE	CC Chen
CHECK	CC Chen
DESIGN	Anderson

DWG.TITLE

11.2 Unpacking the display



12. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.