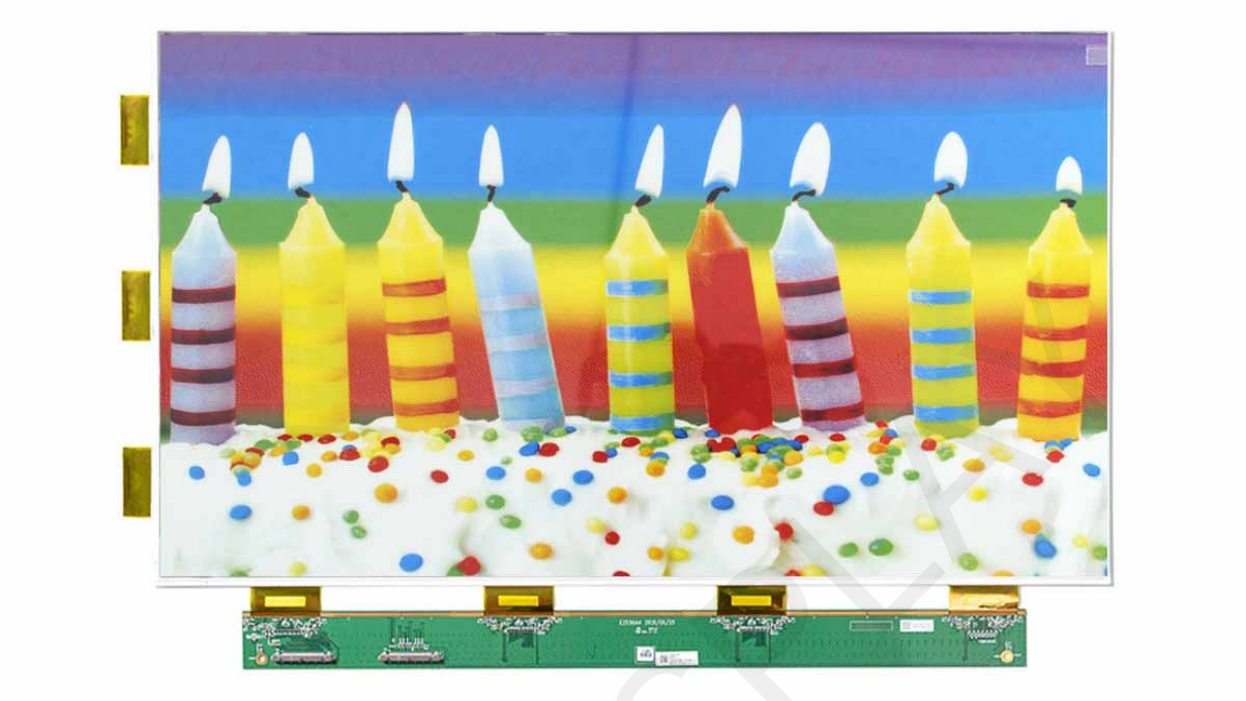
GooDisplay

25.3 inch
E-paper Display Series
GDEP253C02

GooDisplay®

Dalian Good Display Co., Ltd.

Product Specifications



Customer	**Standard**
Description	**25.3" E-PAPER DISPLAY**
Model Name	**GDEP253C02**
Date	**2024/07/22**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
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CONTENTS

1. General Description

GDEP253C02 is a reflective electrophoretic E Ink® Spectra 6 technology display module based on active matrix TFT substrate. It has 25.3” active area with 3200 x 1800 pixels and 16 : 9 aspect ratios. The display is capable to display images at Black/White/Red/ Yellow/Blue/Green depending on the display controller and the associated waveform file it used.

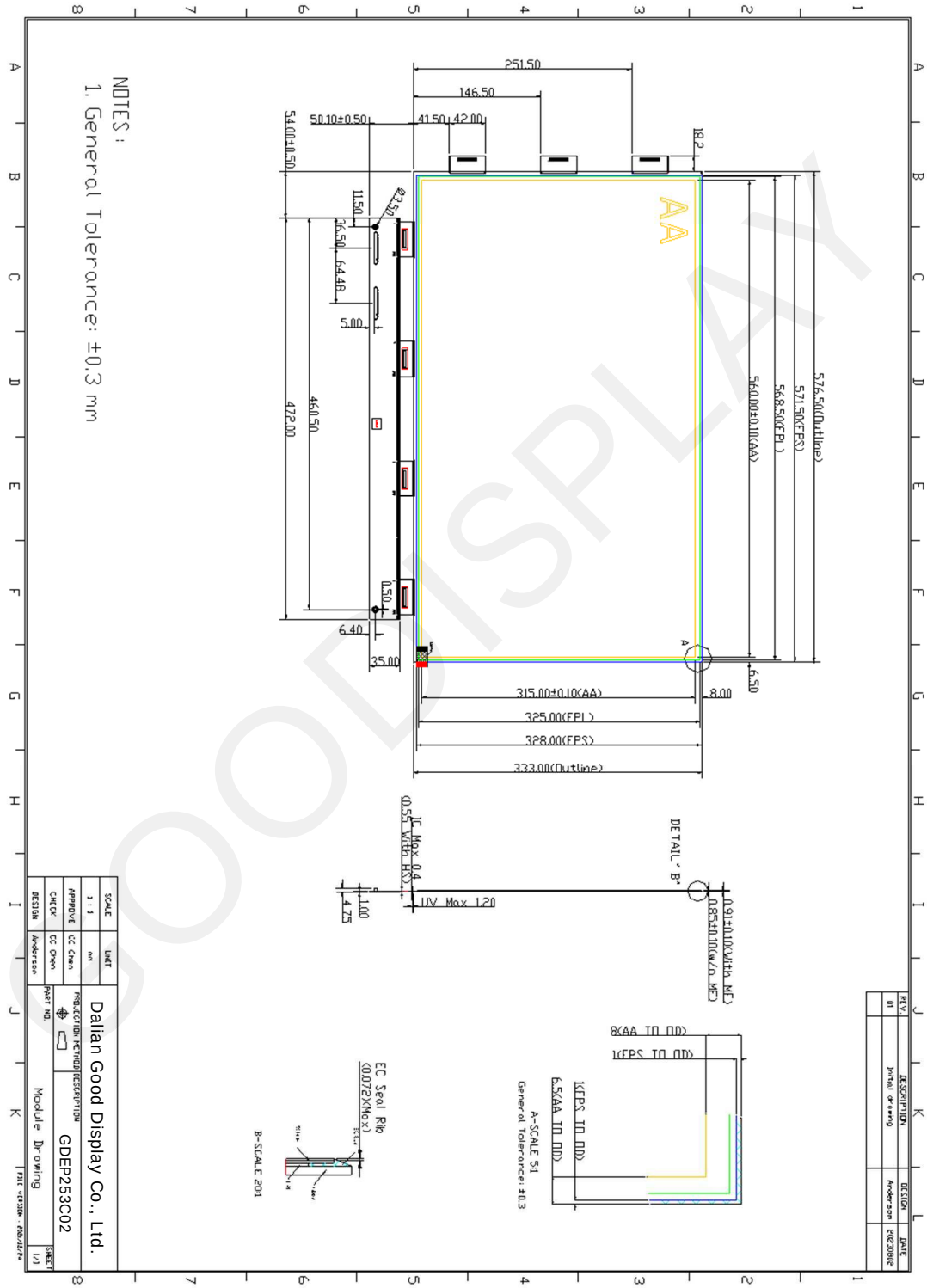
2. Features

- Display Black/White/Red/Yellow/Blue/Green colors
- High contrast
- High reflectance
- Ultra-wide viewing angle
- Pure reflective mode
- Bi-stable image
- Operating temperature range (0 ~ 50 ^{o}C)
- Landscape mode

3. General Specifications

Parameter	Specifications	Unit	Remark
Screen Size	25.3	Inch	
Display Resolution	3200(H) x 1800(V)	Pixel	16:9
Active Area	560.0(H) x 315.0(V)	mm	
Pixel Pitch	0.175(H) x 0.175(V)	mm	
Pixel Configuration	Square		
Outline Dimension	576.5(W) × 333.0(H) × 0.85(D)	mm	w/o masking film
Module Weight	385 ± 15	g	w/ masking film
Display operating mode	Reflective mode		
FPL	E Ink Spectra 6		
Surface treatment	Anti-glare		
Operating Temp. Range	0 ~ 50	°C	
Storage Temp. Range	-25 ~ 60	°C	

4. Mechanical Drawing of Display Module



5. Input / Output Interface

5.1. Pin Assignment

Connector CN1

Pin #	Signal	I/O	Description	Remark
1	VCOM	P	Common Voltage.	
2	VCOM	P	Common Voltage.	
3	VCOM	P	Common Voltage.	
4	NC	-	NO Connection	
5	VCOM	P	Common Voltage.	
6	VCOM	P	Common Voltage.	
7	NC	-	NO Connection	
8	BORDER	P	Border connection	
9	NC	-	NO Connection	
10	VGH	P	Positive power supply gate driver.	
11	VGH	P	Positive power supply gate driver.	
12	NC	-	NO Connection	
13	VP3	P	Positive power supply source driver.	
14	VP3	P	Positive power supply source driver.	
15	VP3	P	Positive power supply source driver.	
16	NC	-	NO Connection	
17	VP2	P	Positive power supply source driver.	
18	VP2	P	Positive power supply source driver.	
19	VP2	P	Positive power supply source driver.	
20	NC	-	NO Connection	
21	VP1	P	Positive power supply source driver.	
22	VP1	P	Positive power supply source driver.	
23	VP1	P	Positive power supply source driver.	
24	NC	-	NO Connection	
25	VDD	P	Logic power.	
26	VDD	P	Logic power.	
27	NC	-	NO Connection	
28	VSS	P	Ground	
29	VSS	P	Ground	
30	NC	-	NO Connection	
31	VN1	P	Negative power supply source driver.	
32	VN1	P	Negative power supply source driver.	

33	VN1	P	Negative power supply source driver.	
34	NC	-	NO Connection	
35	VN2	P	Negative power supply source driver.	
36	VN2	P	Negative power supply source driver.	
37	VN2	P	Negative power supply source driver.	
38	NC	-	NO Connection	
39	VN3	P	Negative power supply source driver.	
40	VN3	P	Negative power supply source driver.	
41	VN3	P	Negative power supply source driver.	
42	NC	-	NO Connection	
43	VGL	P	Negative power supply gate driver.	
44	VGL	P	Negative power supply gate driver.	
45	NC	-	NO Connection	
46	NC	-	NO Connection	
47	NC	-	NO Connection	
48	NC	-	NO Connection	
49	STBYB	I	mini-LVDS enable.	
50	XON	I	XON signal gate driver	
51	MODE	I	Output enable gate driver	

Note: P in I/O: Power pin

Connector CN2

Pin #	Signal	I/O	Description	Remark
1	DSEL	I	Data Input select	
2	LEH	I	Latch enable source driver	
3	OEH	I	Outputs enabled when OE is logic “H”, Outputs forced to GND when OE is logic “L”.	
4	UD	I	Shift direction control pin gate driver UD = H: Data shift direction from G1 to G800. UD = L: Data shift direction from G800 to G1.	
5	SHR	I	Shift direction control pin source driver SHR =H: Data inputs read sequentially from S800 to S1. SHR =L: Data inputs read sequentially from S1 to S800.	
6	SPV2	I/O	Start pulse gate driver UD / Start pulse input / Start pulse output H / SPV1 / SPV2 L / SPV2 / SPV1	

7	SPV1	I/O	Start pulse gate driver UD: H → Start pulse input: SPV1 → Start pulse output: SPV2 UD: L → Start pulse input: SPV2 → Start pulse output: SPV1	
8	SPH2	I/O	Start pulse source driver SHR: H → Start pulse input: SPH2 → Start pulse output: SPH1 SHR: L → Start pulse input: SPH1 → Start pulse output: SPH2	
9	SPH1	I/O	Start pulse source driver SHR: H → Start pulse input: SPH2 → Start pulse output: SPH1 SHR: L → Start pulse input: SPH1 → Start pulse output: SPH2	
10	VSS	P	Ground	
11	CKV	I	Clock gate driver	
12	VSS	P	Ground	
13	LV11N	I	Data signal source driver	
14	LV11P	I	Data signal source driver	
15	VSS	P	Ground	
16	LV10N	I	Data signal source driver	
17	LV10P	I	Data signal source driver	
18	VSS	P	Ground	
19	LV9N	I	Data signal source driver	
20	LV9P	I	Data signal source driver	
21	VSS	P	Ground	
22	LV8N	I	Data signal source driver	
23	LV8P	I	Data signal source driver	
24	VSS	P	Ground	
25	LV7N_D15	I	Data signal source driver	
26	LV7P_D14	I	Data signal source driver	
27	VSS	P	Ground	
28	LV6N_D13	I	Data signal source driver	
29	LV6P_D12	I	Data signal source driver	
30	VSS	P	Ground	
31	CLKN_GLOSTL	I	Data signal source driver	
32	CLKP_CKH	I	Data signal source driver	
33	VSS	P	Ground	
34	LV5N_D11	I	Data signal source driver	

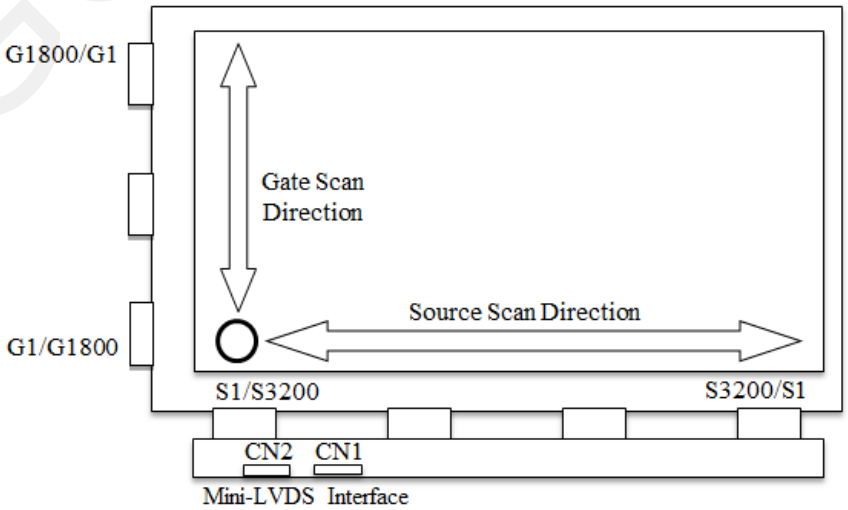
35	LV5P_D10	I	Data signal source driver	
36	VSS	P	Ground	
37	LV4N_D9	I	Data signal source driver	
38	LV4P_D8	I	Data signal source driver	
39	VSS	P	Ground	
40	LV3N_D7	I	Data signal source driver	
41	LV3P_D6	I	Data signal source driver	
42	VSS	P	Ground	
43	LV2N_D5	I	Data signal source driver	
44	LV2P_D4	I	Data signal source driver	
45	VSS	P	Ground	
46	LV1N_D3	I	Data signal source driver	
47	LV1P_D2	I	Data signal source driver	
48	VSS	P	Ground	
49	LV0N_D1	I	Data signal source driver	
50	LV0P_D0	I	Data signal source driver	
51	VSS	P	Ground	

Note: P in I/O: Power pin

5.2. Panels Electrical Connection

SERVICE	CONNECTOR	TYPE NUMBER	NUMBER OF PINS	MATING CONNECTOR
mini-LVDS	CON1	P-TWO 187059-51221 compatible	51	P-TWO 187059-51221 compatible
	CON2	P-TWO 187059-51221 compatible	51	P-TWO 187059-51221 compatible

5.3. Panel Scan Directions



6. Display Module Electrical Characteristics

6.1. Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VDD	-0.3 to +5	V
Positive Supply Voltage	VP3	-0.3 to VN3+50	V
	VP2	-0.3 to VP3	V
	VP1	-0.3 to VP3	V
Negative Supply Voltage	VN1	VN3 to + 0.3	V
	VN2	VN3 to + 0.3	V
	VN3	-25 to + 0.3	V
Supply Voltage	VGH	-0.3 to +55	V
Supply Voltage	VGL	-32 to +0.3	V
Supply Range	VGH-VGL	-0.3 to +55	V

Note

- Maximum ratings are those values beyond which damages to the device may occur.
- Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

6.2. Panel DC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	VSS			0		V
Logic voltage supply	VDD		2.7	3.3	3.6	V
	IDD	VDD=3.3V		15	28	mA
Gate negative supply	VGL		-21	-20	-19	V
	IGL	VGL=-20V		7	8	mA
Gate positive supply	VGH		26	27	28	V
	IGH	VGH=27V		5	6	mA
Source negative supply	VN1		-14	Adjusted	-5	V
	IN1	VN1 = -11.2V		3	25	mA
Source negative supply	VN2		-14	Adjusted	-5	V
	IN2	VN2 = -11V		3	27	mA
Source negative supply	VN3		-16	-15	-14	V
	IN3	VN3 = -15V		5	223	mA
Source positive supply	VP1		5	Adjusted	14	V

	IP1	VP1 = 7.4V		3	5	mA
Source positive supply	VP2		5	Adjusted	14	V
	IP2	VP2 = 6.6V		2	38	mA
Source positive supply	VP3		14	15	16	V
	IP3	VP3 = 15V		4	234	mA
Border supply	-		-	-	-	V
Common voltage	VCOM		-3.5	Adjusted	-0.3	V
	ICOM			12	12	mA
Maximum power panel	Pmax				8136	mW
Typical power panel	Ptyp			607		mW
Standby power panel	Pstby			67		mW
Maximum Currents (*Note 5)	IDD	VDD=3.3V	-300		350	mA
	IGL	VGL=-20V	-850		850	mA
	IGH	VGH=27V	-600		850	mA
	IN1	VN1=-11.2V	-800		800	mA
	IN2	VN2=-11V	-400		900	mA
	IN3	VN3=-15V	-200		1550	mA
	IP1	VP1=7.4V	-600		450	mA
	IP2	VP2=6.6V	-650		850	mA
	IP3	VP3=15V	-400		1500	mA
	ICOM	VCOM=-2V	-400		400	mA

6.3. Panel DC Characteristics for Device Battery-Life Estimation

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	VSS			0		V
Logic voltage supply	VDD		2.7	3.3	3.6	V
	IDD	VDD=3.3V		15	28	mA
Gate negative supply	VGL		-21	-20	-19	V
	IGL	VGL=-20V		7	8	mA
Gate positive supply	VGH		26	27	28	V
	IGH	VGH=27V		5	6	mA
Source negative supply	VN1		-14	Adjusted	-5	V
	IN1	VN1 = -11.2V		3	25	mA
Source negative supply	VN2		-14	Adjusted	-5	V
	IN2	VN2 = -11V		3	27	mA

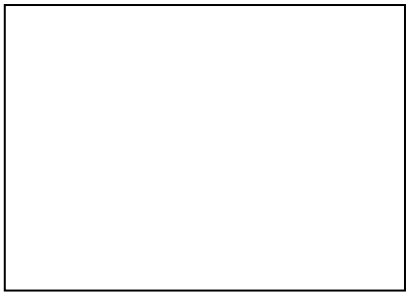
Source negative supply	VN3		-16	-15	-14	V
	IN3	VN3 = -15V		5	121	mA
Source positive supply	VP1		5	Adjusted	14	V
	IP1	VP1 = 7.4V		3	5	mA
Source positive supply	VP2		5	Adjusted	14	V
	IP2	VP2 = 6.6V		2	38	mA
Source positive supply	VP3		14	15	16	V
	IP3	VP3 = 15V		4	114	mA
Border supply	-		-	-	-	V
Common voltage	VCOM		-3.5	Adjusted	-0.3	V
	ICOM			12	12	mA
Maximum power panel	Pmax				4658	mW
Typical power panel	Ptyp			607		mW
Standby power panel	Pstby			67		mW
Maximum Currents (*Note 5)	IDD	VDD=3.3V	-300		350	mA
	IGL	VGL=-20V	-850		850	mA
	IGH	VGH=27V	-600		850	mA
	IN1	VN1=-11.2V	-800		800	mA
	IN2	VN2=-11V	-400		900	mA
	IN3	VN3=-15V	-200		1550	mA
	IP1	VP1=7.4V	-600		450	mA
	IP2	VP2=6.6V	-650		850	mA
	IP3	VP3=15V	-400		1500	mA
	ICOM	VCOM=-2V	-400		400	mA

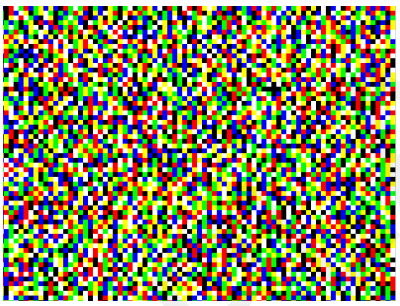
Note

1. The maximum average current for power consumption is measured using 50Hz waveform with following pattern transition: Equivalent to each pixel of ink emerging from continuous white. (Note 6-1)
2. The Typical average current for power consumption is measured using 50 Hz waveform with following pattern transition: from horizontal 6 color scale pattern to vertical 6 color scale pattern.
   (Note 6-2)
3. The standby power is the consumed power when the panel controller is in standby mode.
4. The listed electrical/optical characteristics10are only guaranteed under the controller and waveform provided by Good Display.
5. Vcom is recommended to be set in the range of assigned value ± 0.1 V

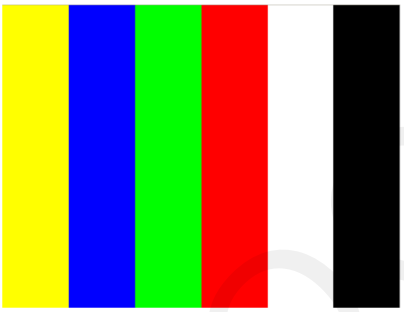
6. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3024)
7. The maximum current is for reference only.
8. The measurement range of power consumption in 6-2) Panel DC characteristics is following the maximum current time. (Note 6-4)
9. The measurement range of power consumption in 6-3) Panel DC Characteristics for Device Battery-Life Estimation is following the full update time. (Note 6-5)

Note 6-1
The Maximum power consumption





Note 6-2
The typical power consumption

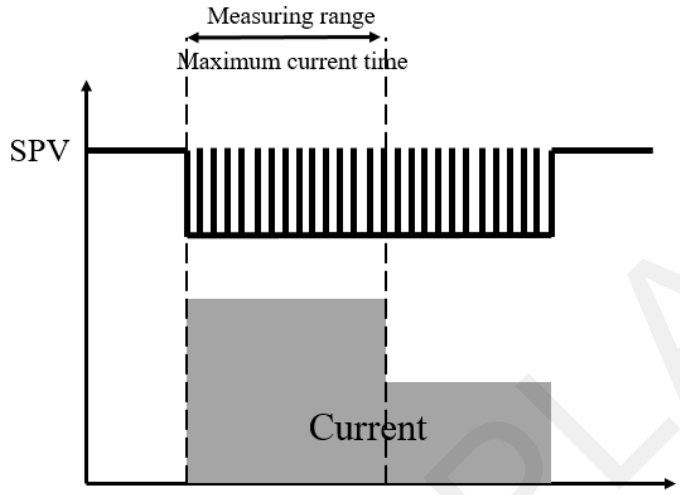


Note 6-3
The decoupling capacitors on each power rail for Max. Currents

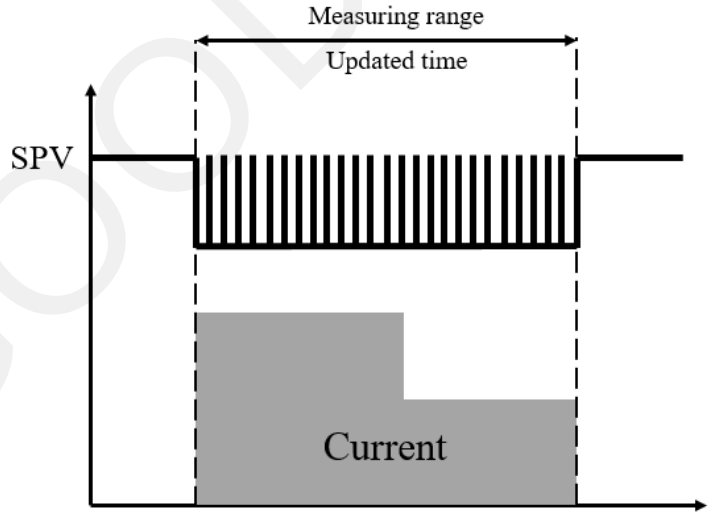
Power rail	Capacitors suggested (uF / Tolerance)
IDD	2.2uF x 14pcs / ±10%
IP1	2.2uF x 12pcs / ±10%
IP2	2.2uF x 12pcs / ±10%
IP3	2.2uF x 12pcs / ±10%
IN1	2.2uF x 12pcs / ±10%
IN2	2.2uF x 12pcs / ±10%
IN3	2.2uF x 12pcs / ±10%
IGH	2.2uF x 2pcs / ±10%
IGL	2.2uF x 3pcs / ±10%

ICOM	No Capacitor

Note 6-4
Schematic diagram of current measurement range in 6-2) Panel DC characteristics.



Note 6-5
Schematic diagram of current measurement range in 6-3) Panel DC Characteristics for Device Battery-Life Estimation.



6.4. Refresh Rate

The module EL253EW1 is applied at a maximum screen refresh rate of 50Hz.

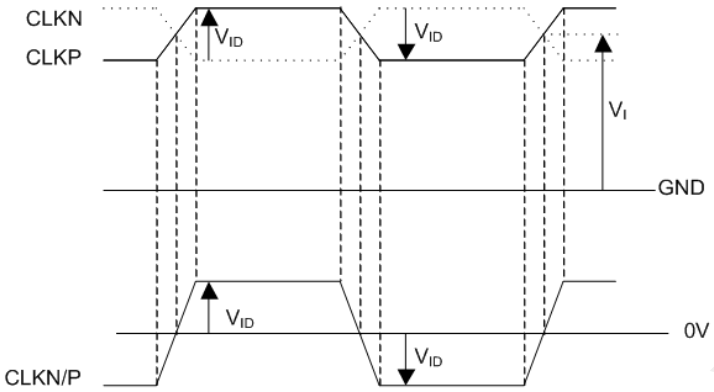
	Min	Max
Refresh Rate	-	50Hz

6.5. Panel AC characteristics

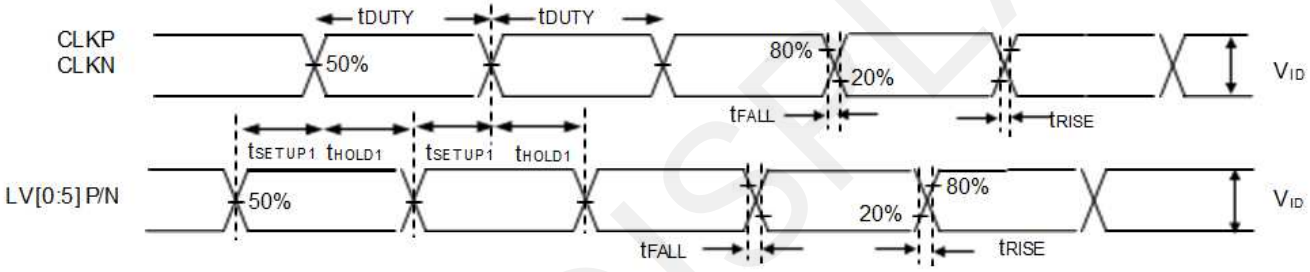
VDD=2.7V to 3.6V, unless otherwise specified.

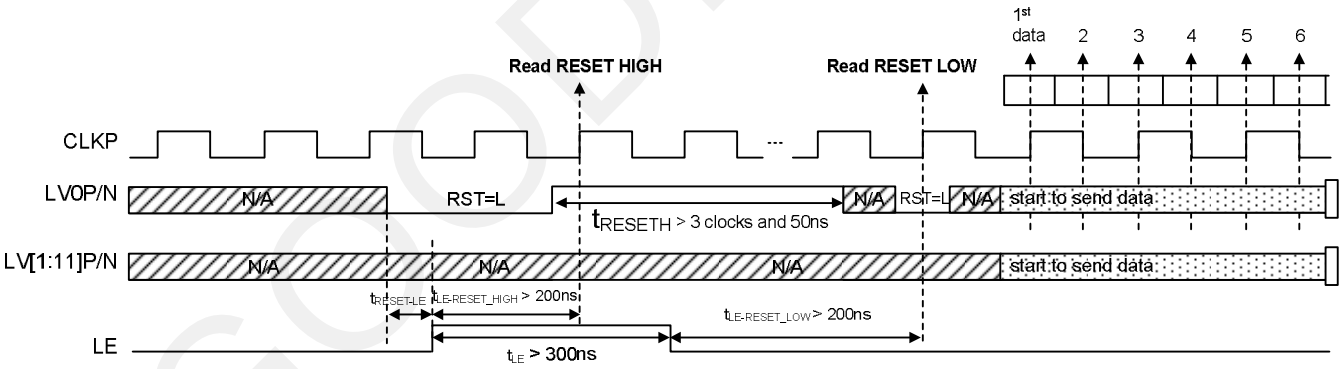
Parameter	Symbol	Min.	Typ.	Max.	Unit
mini-LVDS differential voltage	V_{ID}	300	-	-	mV
mini-LVDS common mode input voltage range	V_I	0.4	1.0	VDD-1.4	V
Source Clock frequency	F_{CLK}	-	-	150	MHz
Source Clock setup time	t_{SETUP1}	1.1	-	-	ns
Source Clock hold time	t_{HOLD1}	1.1	-	-	ns
Rise time	t_{RISE}	-	-	0.15	Unit interval
Fall time	t_{FALL}	-	-	0.15	Unit interval
LE rising to reset input time	$t_{LE\text{-}RESET\_HIGH}$	200	-	-	ns
LE falling to reset input time	$t_{LE\text{-}RESET\_LOW}$	200	-	-	ns
Reset high period	t_{RESETH}	3	-	-	CLK
Receiver off to LE timing	$t_{REC\text{-}OFF}$	40	-	-	CLK
LE width	t_{LE}	300	-	-	ns
Gate clock pulse high period	t_{CLKH}	500	-	-	ns
Gate clock pulse low period	t_{CLKL}	500	-	-	ns
Gate clock rise time	t_{IR_CLK}	-	-	100	ns
Gate clock fall time	t_{IF_CLK}	-	-	100	ns
Gate Start pulse setup time	t_{SU}	100	-	t_{CLKH}-100	ns
Gate Start pulse hold time	t_{HD}	100	-	t_{CLKL}-100	ns
Gate Start pulse rise time	t_{IR_STV}	-	-	100	ns
Gate Start pulse fall time	t_{IF_STV}	-	-	100	ns

Mini-LVDS clock

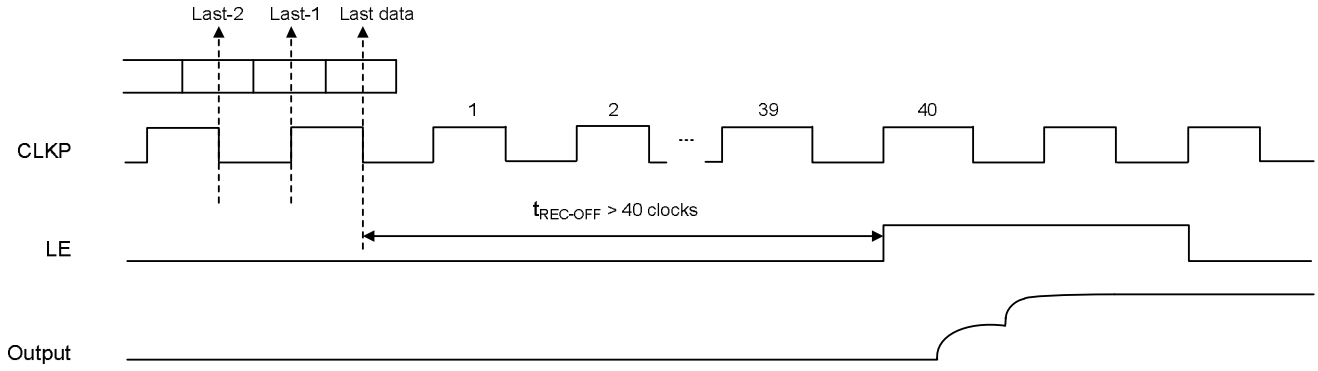


Mini-LVDS timing for receiving data

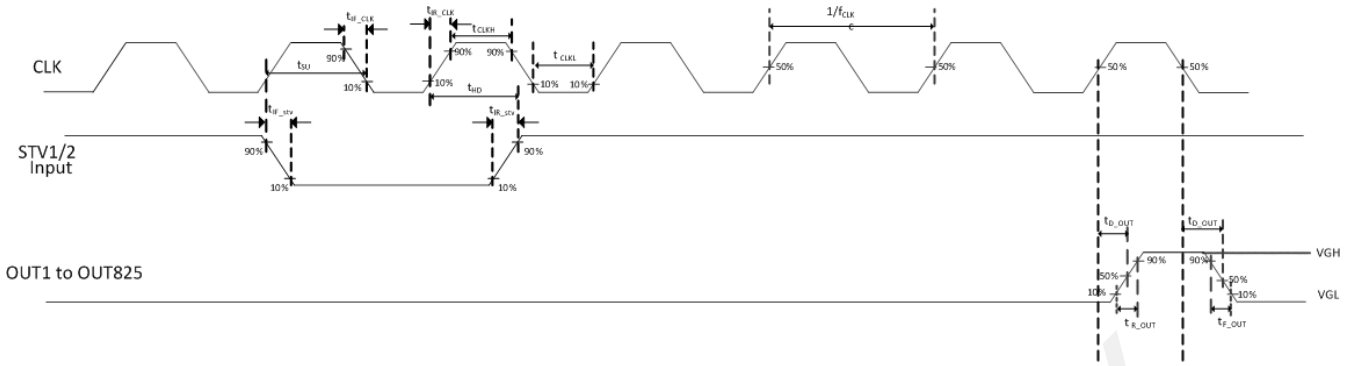




Mini-LVDS last data sampling to LE timing



GATE OUTPUT TIMING



Note : First gate line on timing
After 5CLK, Gate OUT1 is on.

6.6. Controllers Timing

The timing mode is depicted on Figure 6-1 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, the controller timing in the mode LGON follows GDCK timing.

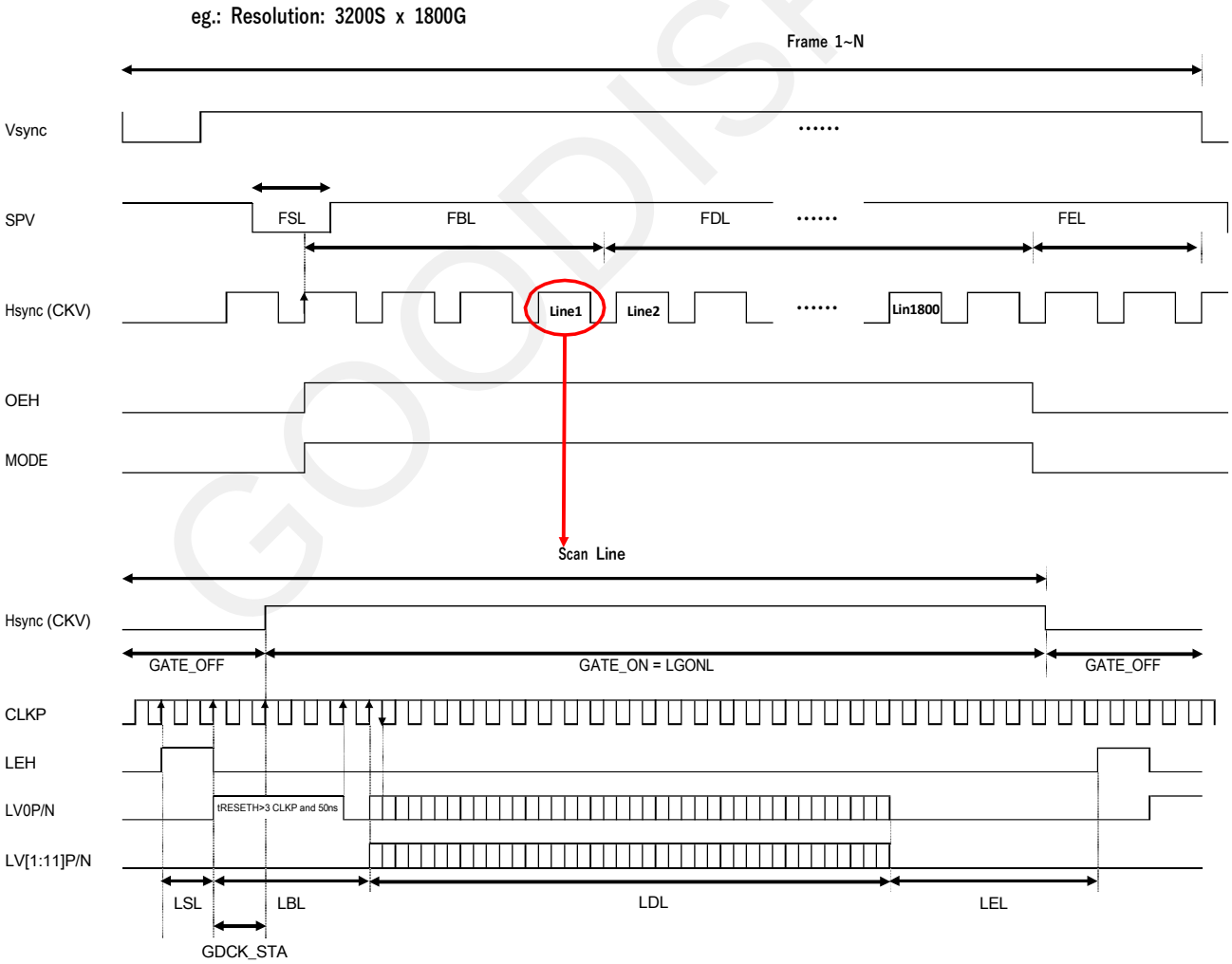


Figure 6-1 Timing in Mode 3

Timing Parameters Table

Mode	3	Resolution 3200 X 1800				
SDCK[MHz]	42					
Pixels per SDCK	8					
Line parameters[SDCK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
	14	10	400	40	3	378
line parameters[us]	-	-	-	-	-	-
	0.33	0.24	9.52	0.95	0.07	9
Frame parameters[lines]	FSL	FBL	FDL	FEL		FR[Hz]
	1	4	1800	5		50
Frame parameters[us]	-	-	-	-	-	-
	11.04	44.16	19872	55.2		19982.4

Note 1: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL

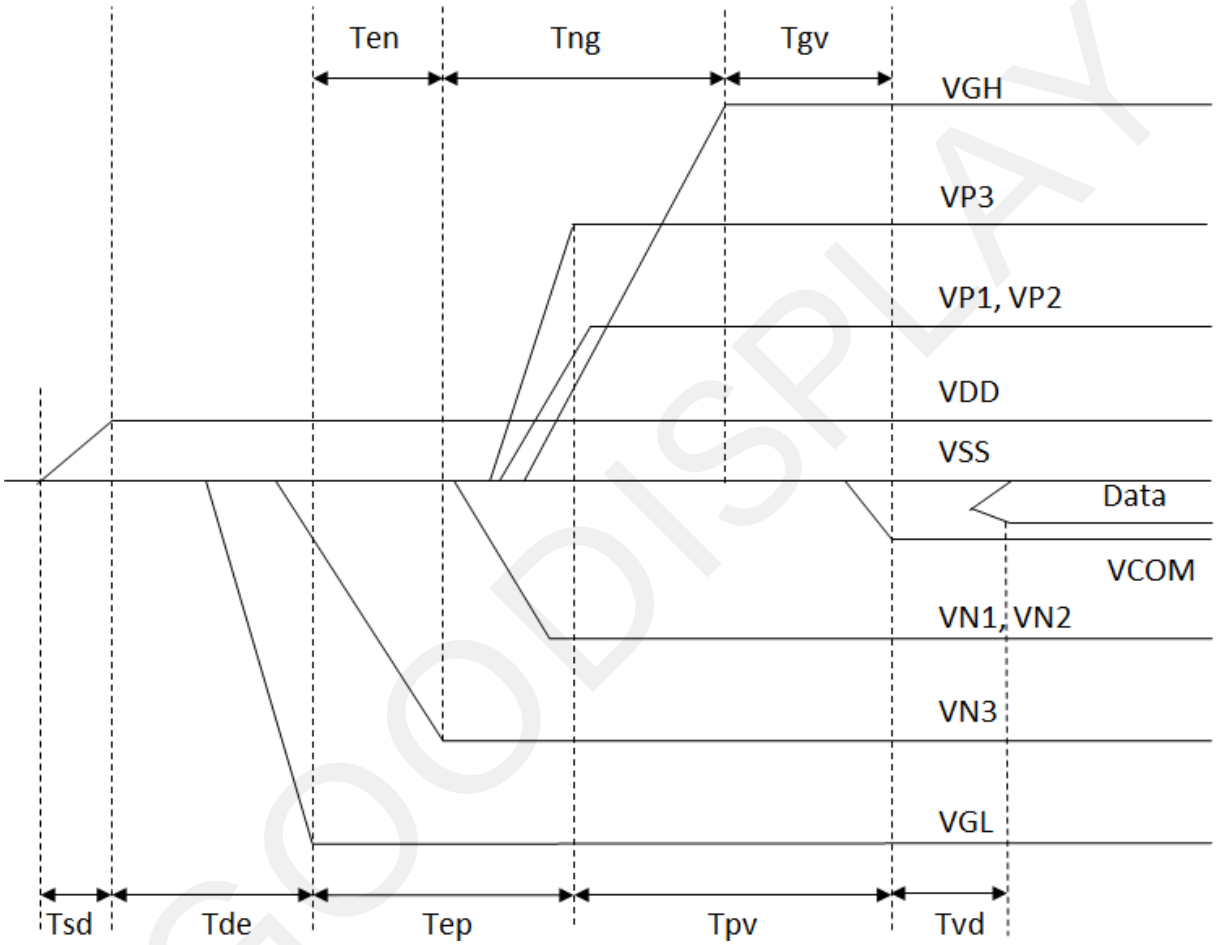
Note 2:
SDCLK = XCL
LV[0:11]P/N = LV0P~LV11N
SDCE_L = XSTL
GDCK = CKV
GDSP = SPV
GDOE = Mode1
SDOE = XOE

7. Power Sequence

Power Rails must be sequenced in the following order :

1. VSS →VDD →VN3 →VN1(VN2) →VP1(VP2) →VP3 →VCOM
2. VSS →VDD →VGL →VGH (Gate driver)

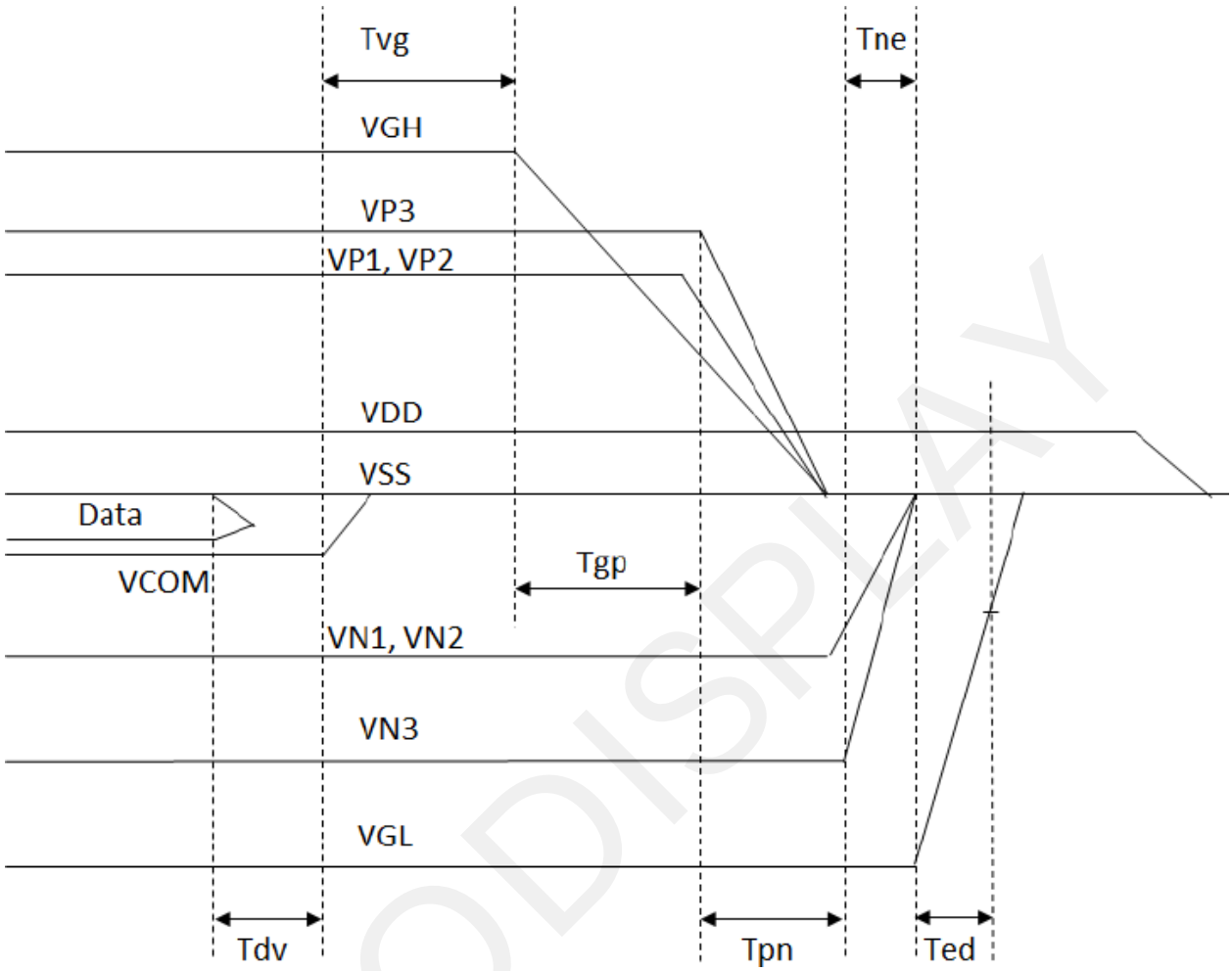
POWER ON



	Min	Max
Tsd	30us	-
Tde	100us	-
Tep	1000us	-
Tpv	100us	-
Tvd	100us	-
Ten	0us	-
Tng	1000us	-

Tgv	100us	-

POWER OFF



	Min	Max	Remark
Tdv	100μs	-	-
Tvg	0μs	-	-
Tgp	0μs	-	-
Tpn	0μs	-	-
Tne	0μs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

8. Optical Characteristics

8.1. Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Temperature	Min	Typ.	Max	Unit	Note
R	Reflectance	White	25°C	30	34	-	%	Note 8-1
CR	Contrast Ratio	-	25°C	15	22	-	-	-
T_{update}	Update time	-	25°C	-	15	-	sec	-
Symbol	Parameter	Conditions	Temperature	L* Typ.	a* Typ.	b* Typ.	△E2000 Max.	Note
WS	White State L*/a*/b* value	White	25°C	66.5	-4	0	6	Note 8-1
DS	Dark State L*/a*/b* value	Dark	25°C	12	7	-11	6	Note 8-1
RS	Red State L*/a*/b* value	Red	25°C	26.5	41	30	6	Note 8-1
YS	Yellow State L*/a*/b* value	Yellow	25°C	62	-11	65	6	Note 8-1
BS	Blue State L*/a*/b* value	Blue	25°C	34	3.5	-37	6	Note 8-1
GS	Green State L*/a*/b* value	Green	25°C	35	-22	15	8	Note 8-1

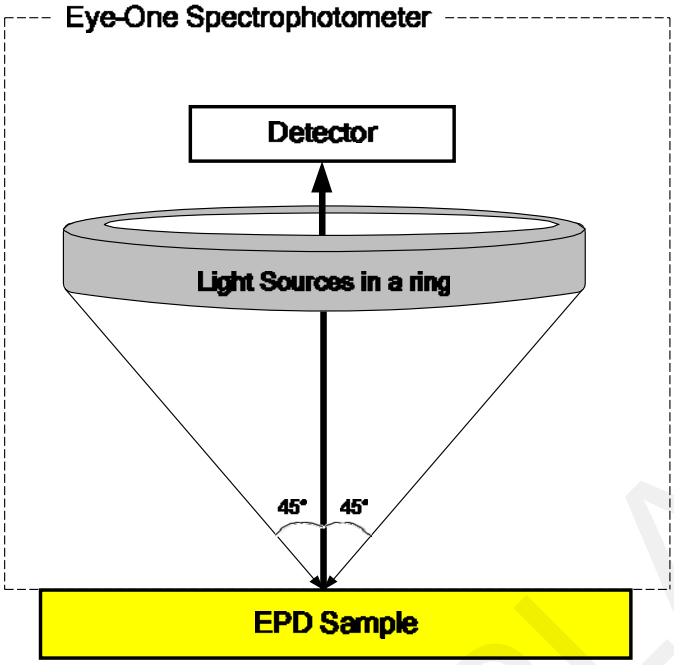
WS: White state, DS: Dark state, RS: Red state, YS: Yellow state, BS: Blue state, GS: Green state

Note 8-1 : Luminance meter : Eye-One Pro3 plus Spectrophotometer

8.2. Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd) :

$$CR = Rl/Rd$$



8.3. Reflection Ratio

The reflection ratio is expressed as :

$$R = \text{Reflectance Factor}_{\text{white board}} \times \left(L_{center} / L_{white\ board} \right)$$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{white\ board}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

10. Reliability Test

#	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% , for 240 hrs 150s interval between updates	IEC 60 068-2-2Be	--
2	Low-Temperature Operation	T = 0°C , for 240 hrs 150s interval between updates	IEC 60 068-2-2Ae	--
3	High Temperature Storage	T = +60°C, RH=35% , for 240 hrs Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25°C , for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% , for 240 hrs 150s interval between updates	IEC 60 068-2-78	
6	High Temperature High Humidity Storage	T = +60℃, RH=80% , for 240 hrs Test in white pattern	IEC 60 068-2-78	
7	Temperature Cycle	-25℃ (30min) → +60℃ (30min), 50 Cycles Test in white pattern	IEC 68-2-14 Nb	--
8	Electrostatic Effect (non-operating)	(Machine model)+/- 250V, 0Ω, 200pF	IEC 62180	
9	Package Vibration	Random Wave (1.5Grms) Frequency: 10~200Hz Direction: X,Y,Z Duration: 30mins each direction	-	Full packed for shipment
10	Package Drop Impact	Height : 33 cm 1 Corner , 3 Edges & 6 Faces	ASTM D 4169&5276 Level 2	Full packed for shipment

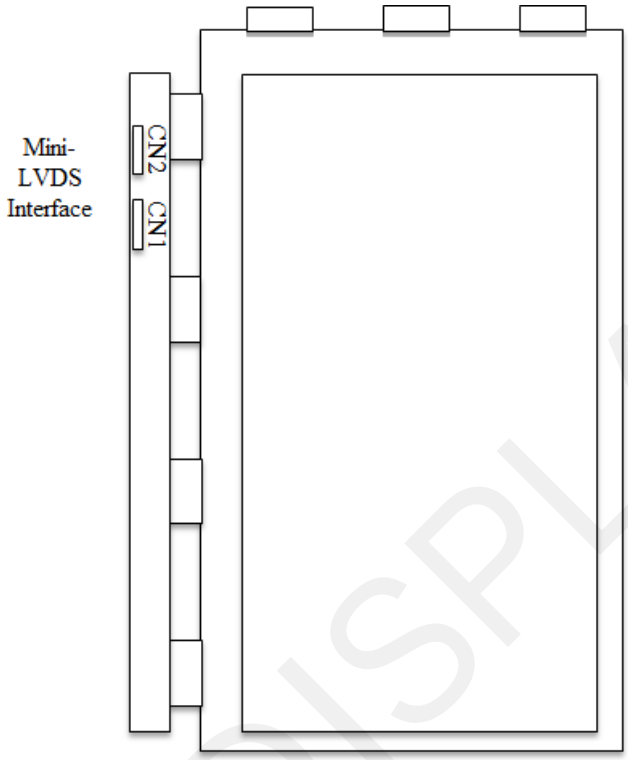
Actual EMC level to be measured on customer application

Note:

1. The protective film must be removed before temperature test.
2. Operation test, 150 seconds interval between image updates.

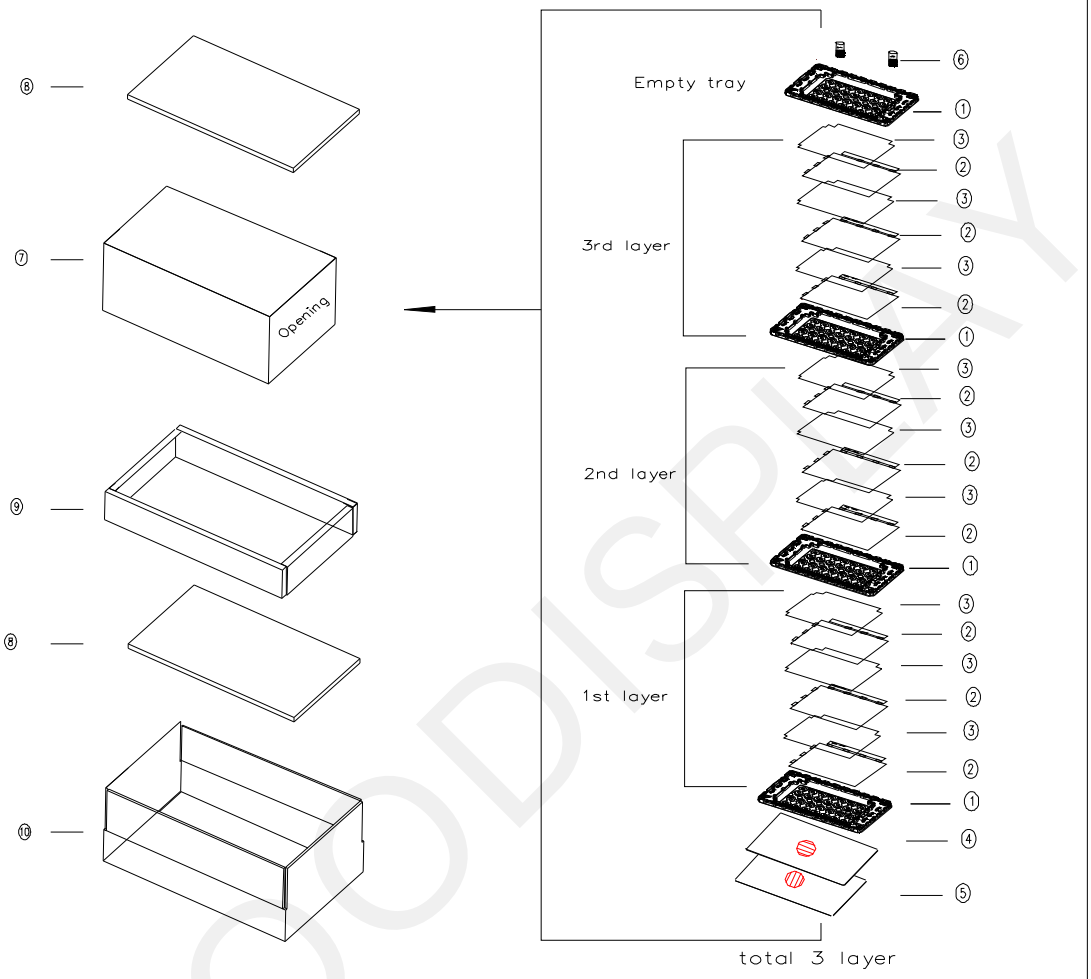
< Criteria >
In the standard conditions, there is not display function NG issue occurred. (including: line defect, no image). All the cosmetic specification is judged before the reliability stress.

11. Block Diagram



12. Packing

REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	Anderson	20230802



ITEM	DESCRIPTION	Q'TY	REMARK
10	CARTON	1	
9	SIDE EPE	1	
8	U_D EPE	2	
7	FOLDED BAG	1	ANTISTATIC
6	30g乾燥劑	2	
5	PP BOARD	1	
4	PP BOARD	1	
3	EPE	9	ANTISTATIC
2	EPD	9	
1	TRAY	4	ANTISTATIC

NOTE:
1. One layer include:
   3 pcs module /1 piece of tray
2. Q'TY: 9 pcs panel/carton
3. Dimension: 550*900*210mm

APPROVE	CC Chen
CHECK	CC Chen
DESIGN	Anderson

DWG.TITLE

13. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. https://www.good-display.com/news/80.html