SSD2680A

Product Proposal

176 Source x 296 Gate
Active Matrix EPD Display Driver with Controller
for color application

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This document contains information on a product under definition stage. Solomon Systech reserves the right to change or discontinue this product without notice.

Appendix: Revision history

Revision	Description of any change	Effective
SSD2680A Product Proposal 0.10	• Initial release of product proposal 0.10	03-Sep-2024
SSD2680A Product Proposal 0.20	• Updated command table	13-Jan-2025

CONTENTS

TABLES

FIGURES

1 General Description

The SSD2680A is an all-in-one AMEPD driver IC with Controller which can support EPD color application.

It consists of 176 source outputs, 296 gate outputs, 1 VCOM & 1 VBD which can support a maximum display resolution 176 x 296.

SSD2680A embeds oscillator, booster & regulators and selectable Serial Peripheral Interface (3-wire/4-wire) to communicate with general MCU.

2 Features

- Design for dot matrix type active matrix EPD display, support Black/White/Color
- Power supply:
  - VDD: 2.2V to 3.6V
  - VDDIO: Connect to VDD
- On chip display RAM
  - 2bit outputs per pixel to support Black/White/Color
- Resolution: 176 source outputs, 296 gate outputs, 1VBD (for border) and 1 VCOM
  - 176 output source drivers with 4 levels output for black/white/color per pixel:
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame):
      - Mode 0: 0V & VSH1 (+15V) & VSL (-15V) & VSH2 (+3V to +15V)
      - Mode 1: 0V & VSH1 (+3V to +15V) & VSL (-3V to -15V) & VSH2 (+3V to +15V)
    - Source driving output voltage (Voltage step: 100mV)
    - Left and Right shift capability
  - 296 output gate drivers:
    - 2-level outputs (VGH, VGL), Max 40Vp-p
    - Gate driving output voltage (VGH/VGL): +/-20V, +/-17V, +/-15V
    - Up and Down shift capability
  - 1 VBD for border level
    - Same function as the programmable source driver with selected LUT
  - 1 VCOM for Common electrode level
    - DCVCOM: -0.2V to -4V (Voltage step: 100mV)
    - ACVCOM: 4 levels output (DCVCOM, VSH1+DCVCOM, VSL+DCVCOM and floating)
    - Built in VCOM sensing.
- On-chip oscillator
- Programmable output Waveform Settings
- Support frame rate: 120Hz (max)
- Embedded 3840 Bytes MTP to store the waveform settings and parameters
- Support low voltage detect for supply voltage.
- Internal Temperature Sensor of +/-2degC accuracy from -25degC to 50degC, 7-bit status
- MCU interface: Serial peripheral (3-wire/4-wire), Maximum SPI write speed 20MHz
- Available in COG package

3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form	Remark
SSD2680AZ2	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 9um
SSD2680AZA	Gold Bump Die	Bump Face Down On Waffle pack Die thickness: 300um Bump height: 9um

4 Block Diagram

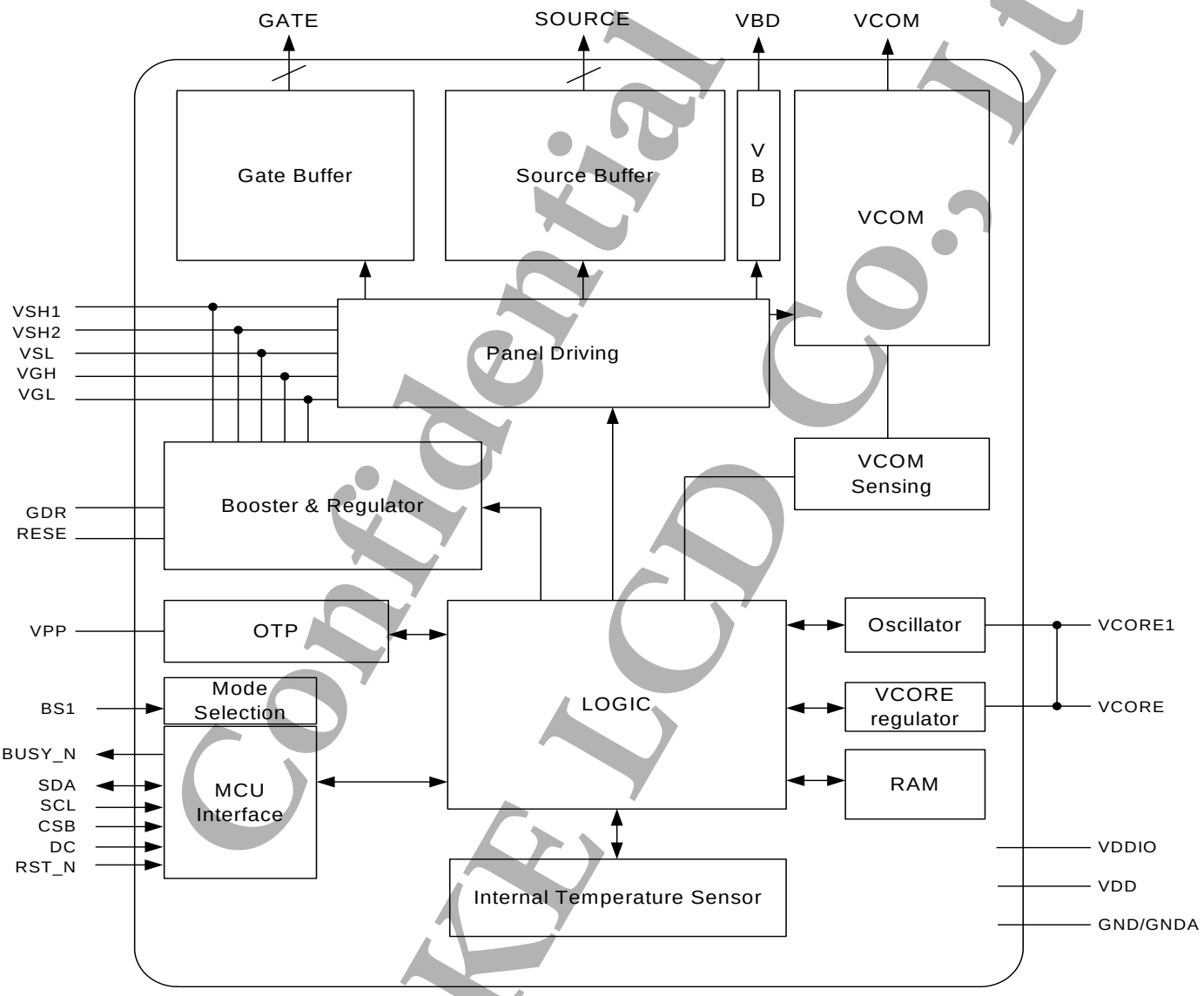


Figure 4-1: SSD2680A Block Diagram

5 PIN DESCRIPTION

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to GND, Pull H = connect to V_{DDIO}

Table 5-1: Power Supply Pins

Name	Type	Connect to	Function	Description	When not in use
VDD	P	Power Supply	Power Supply	Power input pin for the chip.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the interface. - Connect to VDD in the application circuit.	-
VCORE	C	Capacitor	Logic Power	Core logic power pin. VCORE is regulated internally from VDD.	-
VCORE1	C	Capacitor	Logic Power	Core logic power pin1. - connect to VCORE in the application circuit	-
GND	P	GND	GND	**Ground**	-
GNDA	P	GND	GND	Ground - Connect to GND in the application circuit	-
VPP	P	Reserved	Reserved	Reserved Keep it floating.	-

Table 5-2: Interface Logic Pins

Name	Type	Connect to	Function	Description	When not in use
BS1	I	VDDIO/GND	MCU Interface Mode Selection	This pin is for selecting 3-wire or 4-wire SPI bus. BS1: 0 = 4-wire SPI; 1 = 3-wire SPI(9 bits SPI)	-
SCL	I	MPU	Data Bus	Serial clock pin for interface	-
SDA	I/O	MPU	Data Bus	Serial data pin for interface	-
CSB	I	MPU	Logic Control	This pin is the chip select input connecting to the MCU.	-
DC	I	MPU	Logic Control	This pin is Data/Command control pin connecting to the MCU.	VDDIO or GND
RST_N	I	MPU	System Reset	This pin is reset signal input. Active Low.	-
BUSY_N	O	MPU	Device Busy Signal	This pin indicates the driver status. L: Driver is busy **H: non-busy. Host side can send command/data to driver.**	Open
M/S#	NC	NC	Reserved	It can be float or connect to VDDIO/GND.	Open

Table 5-3: Analog Pins

Name	Type	Connect to	Function	Description	When not in use
GDR	O	MOSFET Driver	VGH, VGL Generation	This pin is N-Channel MOSFET gate drive control pin.	-
RESE	I	Booster Control Input		This pin is Current sense input pin for the control Loop.	-
VGH	C	Stabilizing capacitor		This pin is Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and GND in the application circuit.	-
VGL	C	Stabilizing capacitor		This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and GND in the application circuit.	-
VSH1	C	Stabilizing capacitor	VSH1, VSH2, VSL Generation	This pin is Positive Source driving voltage, VSH1 Connect a stabilizing capacitor between VSH1 and GND in the application circuit.	-
VSH2	C	Stabilizing capacitor		This pin is Positive Source driving voltage, VSH2 Connect a stabilizing capacitor between VSH2 and GND in the application circuit.	-
VSL	C	Stabilizing capacitor		This pin is Negative Source driving voltage, VSL. Connect a stabilizing capacitor between VSL and GND in the application circuit.	-
VCOM	C	Panel & Stabilizing capacitor	VCOM driving signal	This pin is VCOM driving volage, VCOM. Connect a stabilizing capacitor between VCOM and GND in the application circuit.	-

Table 5-4: Driver Output Pins

Name	Type	Connect to	Function	Description	When not in use
S [175:0]	O	Panel	Source driving signal	Source output pin.	Open
G [295:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD	O	Panel	Border driving signal	**Border output pin.**	Open

Table 5-5: Other Pins

Name	Type	Connect to	Function	Description	When not in use
TIN	I	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
TPE	O	NC	Reserved for Testing	This is a reserved pin and should be kept open.	Open
GPIO [0:1]	I/O	Open	Reserved	Reserved	Open
CL	I/O	Open	Reserved	Reserved	Open
TPA, TPB, TPC, TPD, TPF, TPG	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Do not connect to other NC pins and test pins including TPA, TPB, TPC, TPD, TPF and TPG.	Open

6 Functional Block Description

6.1 MCU Interface

6.1.1 MCU Interface selection

The SSD2680A can support 3-wire/4-wire serial peripheral. In the SSD2680A, the MCU interface is pin selectable by BS1 shown in Table 6-1.

Table 6-1: Interface pins assignment under different MCU interface

MCU Interface	BS1	RST_N	CSB	DC	SCL	SDA
4-wire serial peripheral interface (SPI)	L	Required	CSB	DC	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	CSB	L	SCL	SDA

Note:

(1) L is connected to GND and H is connected to VDDIO

6.1.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, DC and CSB. The control pins status in 4-wire SPI in reading/writing command/data is shown in

Table 6-2. The read/write procedure of 4-wire SPI is shown in Figure 6-1.

Table 6-2: Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	L	L
Read/Write data	↑	Data bit	H	L

Note:

(1) L is connected to GND and H is connected to VDDIO
(2) ↑ stands for rising edge of signal
(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of DC should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to DC pin.

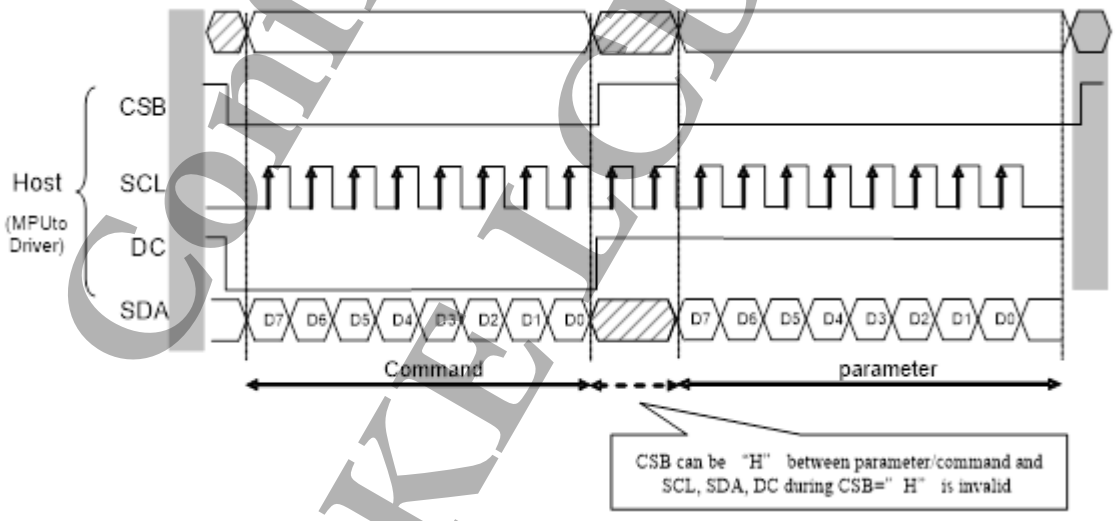


Figure 6-1: Read/Write procedure in 4-wire SPI mode

6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CSB. The operation is similar to 4-wire SPI while DC pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the read/write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is DC bit, D7 bit, D6 bit to D0 bit. The first bit is DC bit which determines the following byte is command or data. When DC bit is 0, the following byte is command. When DC bit is 1, the following byte is data. The read/write procedure of 3-wire SPI is shown in Figure 6-2.

Table 6-3: Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	Tie LOW	L
Read/Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to GND and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

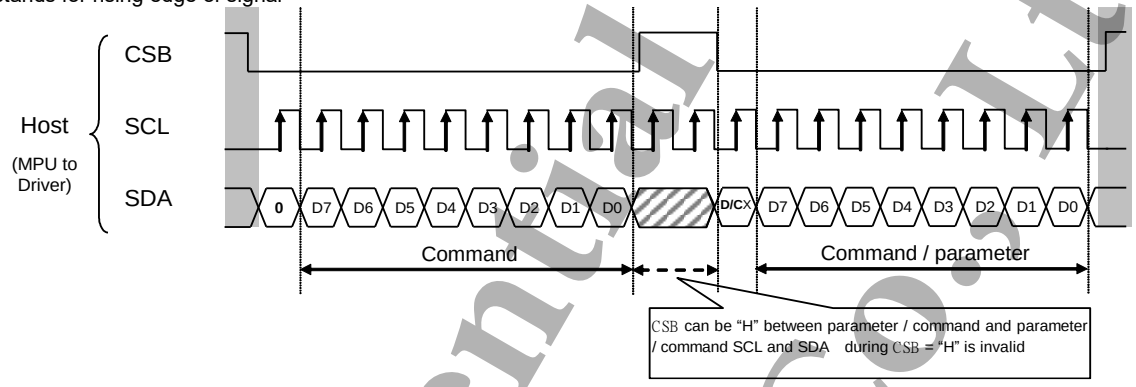


Figure 6-2: Read/Write procedure in 3-wire SPI mode

6.2 RAM

The On-chip display RAM is holding the image data. 2bpp for 176x296 resolution

6.3 Oscillator

The oscillator module generates the clock reference for waveform timing and analog operations.

6.4 Booster & Regulator

A voltage generation system is included in the driver. It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH1, VSH2, VSL and VCOM. External application circuit is needed to make the on-chip booster & regulator circuit work properly.

6.5 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level. The sensed value can be programmed into MTP. It required PON with DCVCOM mode for analog voltage ready.

The typical flow of VCOM sensing:

- Active Gate is scanning during the VCOM sense Period.
- Source are GND.
- VCOM pin is used for sensing.
- During Sensing period, BUSY_N is kept flagged.
- After Sensing, Active Gate return to non-select stage.

7 COMMAND TABLE

7.1 User Command Table

Table 7-1: Summary of user command table

R/W#	DC	Code	Command	D7	D6	D5	D4	D3	D2	D1	D0	POR
W	0	00h	PSR Panel Setting Register	0	0	0	0	0	0	0	0	
W	1			RES[1:0]		B_mode	0	UD	SHL	SHD_N	RST_N	2Fh
W	1			LUT_EN	FOPT[1:0]		VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
W	0	01h	PWR Power setting Register	0	0	0	0	0	0	0	1	
W	1			0	0	BD_EN	Reserved	Reserved	VSC_EN	VS_EN	VG_EN	07h
W	1			1	1	1	1	0	0	VGPN[1:0]		F0h
W	1			0	VSPL[6:0]							00h
W	1			0	VSNL[6:0]							00h
W	1			0	VSPL2[6:0]							00h
W	1			0	VSNL2[6:0]							00h
W	0	02h	POF Power OFF Command Register	0	0	0	0	0	0	1	0	
W	1			00h								-
W	0	03h	POFS Power off Sequence Setting Register	0	0	0	0	0	0	1	1	
W	1			0	0	T_VDPG_OFF[1:0]		0	0	T_VDS_OFF[1:0]		00h
W	0	04h	PON Power ON Command Register	0	0	0	0	0	1	0	0	
W	0	06h	BTST Booster Soft Start Setting Register	0	0	0	0	0	1	1	0	
W	1			0	0	0	0	T_VGHSSA[1:0]		T_VGHSSB[1:0]		0Fh
W	1			0	0	VGHSSA_DRV[5:0]						04h
W	1			0	0	VGHSSA_OFFT[[5:0]						0Bh
W	1			0	0	VGHSSB_DRV[5:0]						10h
W	1			0	0	VGHSSB_OFFT[[5:0]						0Eh
W	1			0	0	VGHSSC_DRV[5:0]						10h
W	1			0	0	VGHSSC_OFFT[[5:0]						05h
W	0	07h	DSLP Deep Sleep Register	0	0	0	0	0	1	1	1	
W	1			A5h								-
W	0	10h	DTM Data Start transmission Register	0	0	0	1	0	0	0	0	
W	1			KPixel1[1:0]		KPixel2[1:0]		KPixel3[1:0]		KPixel4[1:0]		-
W	1			..	..	..	..	..	..	..	..	...
W	1			Kpixel(4M-3)[1:0]		Kpixel(4M-2)[1:0]		Kpixel(4M-1)[1:0]		Kpixel(4M)[1:0]		-
W	0	12h	DRF Display Refresh Command Register	0	0	0	1	0	0	1	0	
W	1			00h								-
W	0	17h	AUTO Auto Sequence Register	0	0	0	1	0	1	1	1	
W	1			A5h or A7h								-
W	0	30h	PLL Frame Rate Control register	0	0	1	1	0	0	0	0	
W	1			0	0	0	0	DYNA		FR[2:0]		02h
W	0	40h	TSC. Temperature Sensor Command Register	0	1	0	0	0	0	0	0	
R	1			TS[7:0]								-
W	0	41h	TSE Temperature Sensor Enable Register	0	1	0	0	0	0	0	1	
W	1			TSE	0	0	0	TO[3:1]			0	00h
W	0	50h	CDI VCOM and DATA interval setting Register	0	1	0	1	0	0	0	0	
W	1			VBD[2:0]			DDX	CDI[3:0]				97h
W	0	51h	LPD Lower Power Detection Register	0	1	0	1	0	0	0	1	
R	1			0	0	0	0	0	0	0	LPDstatus	
W	0	60h	TCON TCON setting Register	0	1	1	0	0	0	0	0	
W	1			S2G[5:0]								04h
W	1			G2S[5:0]								02h
W	0	61h	TRES Resolution setting Register	0	1	1	0	0	0	0	1	
W	1			0	0	0	0	0	0	0	HRES[8]	00h
W	1			HRES[7:0]								B0h
W	1			0	0	0	0	0	0	0	VRES[8]	01h
W	1			VRES[7:0]								28h
W	0	62h	HTOTAL	0	1	1	0	0	0	1	0	
W	1			HTOTAL_A[7:0]								44h
W	1			HTOTAL_B[7:0]								38h
W	0	65h	GSST Gate/Source Start Setting Register	0	1	1	0	0	1	0	1	
W	1			0	0	0	0	0	0	0	S_start[8]	00h
W	1			S_start[7:0]								00h
W	1			0	0	0	0	0	0	0	G_start[8]	00h
W	1			G_start[7:0]								00h

R/W#	DC	Code	Command	D7	D6	D5	D4	D3	D2	D1	D0	POR
W	0	70h	REV Chip Revision Register	0	1	1	1	0	0	0	0	
R	1			A[7:0]								C3h
R	1			B[7:0]								01h
R	1			C[7:0]								01h
W	0	80h	AMV Auto Measurement VCOM Register	1	0	0	0	0	0	0	0	
W	1			P[1:0]		AMVT[1:0]		AMVX	AMVS	0	AMVE	00h
W	0	81h	VV VCOM Value Register	1	0	0	0	0	0	0	1	
R	1			1	0	VV[5:0]						-
W	0	82h	VDCS VCM_DC Setting Register	1	0	0	0	0	0	1	0	
W	1			OTP_VCM	VDCS[6:0]							00h
W	0	83h	PTLW PARTIAL WINDOW	1	0	0	0	0	0	1	1	
W	1			0	0	0	0	0	0	0	HRST[8]	00h
W	1			HRST[7:0]								00h
W	1			0	0	0	0	0	0	0	HRED[8]	00h
W	1			HRED[7:0]								AFh
W	1			0	0	0	0	0	0	0	VRST[8]	00h
W	1			VRST[7:0]								00h
W	1			0	0	0	0	0	0	0	VRED[8]	01h
W	1			VRED[7:0]								27h
W	1			0	0	0	0	0	0	#	PMODE	00h
W	0	90h	PGM Program Mode	1	0	0	1	0	0	0	0	
W	0	91h	APG Active Program	1	0	0	1	0	0	0	1	
W	0	92h	ROTP Read OTP Data	1	0	0	1	0	0	1	0	
R	1			dummy byte								-
R	1			Address 0 in OTP								-
R	1			...								...
R	1			Address n in OTP								-
W	0	93h	RSRAM Read SRAM Data	1	0	0	1	0	0	1	1	
R	1			dummy byte								-
R	1			Address 0 in SRAM								-
R	1			...								...
R	1			Address n in SRAM								-
W	0	A2h	PGM_CFG	1	0	1	0	0	0	1	0	
W	1			0	0	1	1	0	PGM_UMODE[2:0]			31h
W	1			PGM_SADDR[15:8]								00h
W	1			PGM_SADDR[7:0]								00h
W	1			PGM_DSIZE[15:8]								00h
W	1			PGM_DSIZE[7:0]								00h
W	0	A3h	PGM_STAT MTP Program Status	1	0	1	0	0	0	1	1	
R	1			0	0	0	0	0	0	PGM_VER_ERR	PGM_EXE_ERR	00h
W	0	A4h	MTP_STAT MTP Status Register	1	0	1	0	0	1	0	0	
R	1			LUT_TYPE	0	0	0	0	0	0	0	00h
R	1			Reserved[7:0]								00h
R	1			FREE_UI[7:0]								00h
W	0	E0h	CCSET Temperature input selection	1	1	1	0	0	0	0	0	
W	1			0	0	0	0	0	0	TSFIX	0	00h
W	0	E3h	PWS Power Saving Register	1	1	1	0	0	0	1	1	
W	1			VCOM_W[3:0]				SD_W[3:0]				65h
W	0	E4h	LVSEL LVD Voltage Select Register	1	1	1	0	0	1	0	0	
W	1			0	0	0	0	0	0	LVD_SEL[3:0]		03h
W	0	E6h	TSSET Manual input temperature value	1	1	1	0	0	1	0	0	
W	1			TS_SET[7:0]								00h
W	0	E7h	PST	1	1	1	0	0	1	1	1	
W	1			0	0	VGHSM_DRV[5:0]						10h
W	1			0	0	VGHSM_OFFT[[5:0]						05h

Note:

(1) The bit which has been written as “0” or ”1” in Table 7-1 must be followed. Otherwise, device malfunction may occur.
(2) The driver IC will not response to all read & write commands during BUSY_N=0.
(3) Commands are only effective while all corresponding parameters for that command were written completely.
(4) Commands or parameters not shown on above table are for “Reserve” usage.
(5) POR value may be changed without notice.

8 Command Table Description

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register A[7:0] = 2Fh [POR] B[7:0] = 09h [POR]
0	1		A_7	A_6	A_5	0	A_3	A_2	A_1	A_0		A[7:6] ~ RES[1:0] Display Resolution setting (source x gate) 00b: Follow TRES setting: 176 x 296 (Default), Map1 01b: 128 x 296, Map2 10b: 128 x 250, Map2 11b: 112 x 204, Map2 Map1: • Source output from S0 to S175, • RAM byte count as 13024. Map2: • Source output from S8 to S167, • S0~S7, S168~S175, VBD [outer] are HIZ. • RAM byte count as 11840. *Remark: Inactive Gate outputs will be VGL for DRF and AMV. Inactive Source outputs will follow VCOM LUT output for DRF A[5] ~ B_mode Blanking Mode for voltage switching, the duration setting follow CDI. 0: Mode A Blanking time only for ACVCOM. 1: Mode B (Default) Blanking time for ACVCOM or switch mode of source power. A[3] ~ UD Gate Scan Direction: 0: Scan down. First line to Last line: Gn-1 … G0 1: Scan up. (Default) First line to Last line: G0 … Gn-1 A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 … S0 1: Shift right. (Default) First data to Last data: S0 … Sn-1 A[1] ~ SHD_N Booster Switch: 0 : Booster off, register data are kept, and Source/VBD/ Vcom are kept 0V or floating. 1 : Booster on. (Default) A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled. 1: Normal operation (Default). BUSY_N will output low during operation.

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		B[7] ~ LUT_EN 0: During reset, auto load LUT from MTP if it is valid. When PON/DRF, analog setting will follow the content of MTP. (Default) 1: During reset, no action to load LUT from MTP. When PON/DRF, analog setting will follow the content of MCU B[6:5] ~ FOPT[1:0] FOPT function 00b: NO effect. Scan 1 frame after waveform finished (Default) 01b: Will scan 1 frame same as last output (of LUT) after waveform finished. 10b: Will scan 1 frame with Floating output after waveform finished. 11b: No Scan after waveform finished (Power off floating) B[4] ~ VCMZ VCOM Hi-Z option 0: NO effect. (default) 1: VCOM is always floating. B[3] ~ TS_AUTO Temperature Sensor auto option 0: NO effect. 1: Before loading MTP, Temperature Sensor will be activated automatically one time. (default) B[2] ~ TIEG VGL power off option 0: NO effect. (default) 1: After power off booster, VGL will be tied to GND. B[1] ~ NORG VCOM display end GND option 0: NO effect. (default) 1: After refreshing display, VCOM is tied to GND before power off B[0] ~ VC_LUTZ VCOM display end floating option 0: NO effect. 1: After refreshing display, the output of VCOM is set to floating automatically (default)

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>PWR</td><td>Power setting Register
A[5:0] = 07h [POR]
B[7:0] = F0h [POR]
C[6:0] = 00h [POR]
D[6:0] = 00h [POR]
E[6:0] = 00h [POR]
F[6:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td rowspan="6">A[5] ~ BD_EN
Border output level selection:
<table><tr><th>Border level</th><th>BD_EN=0 (default)</th><th>BD_EN=1</th></tr><tr><td>00</td><td>VCOM</td><td>VCOM</td></tr><tr><td>01</td><td>VSH</td><td>VSH+DCVCOM</td></tr><tr><td>10</td><td>VSL</td><td>VSL+DCVCOM</td></tr><tr><td>11</td><td>VSH2</td><td>VSH2+DCVCOM</td></tr></table>
A[4:3] ~ reserved

A[2] ~ VSC_EN
Source LV power selection:
0: External source power for VSH2 pin.
1: Internal DCDC function for generate source power. (default)
A[1] ~ VS_EN
Source LV power selection:
0: External source power for VSH1 and VSL pin.
1: Internal DCDC function for generate source power. (default)
A[0] ~ VG_EN
Gate power selection:
0: External gate power for VGH and VGL pin.
1: Internal DCDC function for generate gate power. (default)

B[1:0] ~ VGPN [1:0]
Internal VGH / VGL Voltage Level Selection:
<table><tr><th>VGPN [1:0]</th><th>Gate Voltage Level</th></tr><tr><td>00</td><td>VGH=20V,VGL=-20V (Default)
VSH=15V, VSL=-15V</td></tr><tr><td>01</td><td>VGH=17V ,VGL=-17V
VSH=15V, VSL=-15V</td></tr><tr><td>10</td><td>VGH=15V,VGL=-15V
VSH=13V, VSL=-13V</td></tr><tr><td>11</td><td>Reserved.</td></tr></table>
C[6:0] ~ VSPL [6:0], Internal Source Voltage Level Selection for VSH2@Mode0.
D[6:0] ~ VSNL[6:0], Internal Source Voltage Level Selection for VSL@Mode1.
E[6:0] ~ VSPL2[6:0], Internal Source Voltage Level Selection for VSH1@Mode1.
F[6:0] ~ VSNL2[6:0], Internal Source Voltage Level Selection for VSH2@Mode1.

Mode0: VSH1=15V, VSL=-15V, VSH2=3~15V
Mode1: VSH1=3~15V, VSL=-3~-15V, VSH2=3~15V
*Remark:
If VGH/VGL <+/-15V,
VSH/VSH2/VSL (max) = (VGH-2V / VGL+2V)</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>B_1</td><td>B_0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>D_6</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>E_6</td><td>E_5</td><td>E_4</td><td>E_3</td><td>E_2</td><td>E_1</td><td>E_0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>F_6</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td><td></td></tr>
</table>

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description

VSPL[6:0]/VSPL2[6:0]/VSNL2[6:0]:

[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage
00h	3V	15h	5.1V	2Ah	7.2V	3Fh	9.3V	54h	11.4V	69h	13.5V
01h	3.1V	16h	5.2V	2Bh	7.3V	40h	9.4V	55h	11.5V	6Ah	13.6V
02h	3.2V	17h	5.3V	2Ch	7.4V	41h	9.5V	56h	11.6V	6Bh	13.7V
03h	3.3V	18h	5.4V	2Dh	7.5V	42h	9.6V	57h	11.7V	6Ch	13.8V
04h	3.4V	19h	5.5V	2Eh	7.6V	43h	9.7V	58h	11.8V	6Dh	13.9V
05h	3.5V	1Ah	5.6V	2Fh	7.7V	44h	9.8V	59h	11.9V	6Eh	14V
06h	3.6V	1Bh	5.7V	30h	7.8V	45h	9.9V	5Ah	12V	6Fh	14.1V
07h	3.7V	1Ch	5.8V	31h	7.9V	46h	10V	5Bh	12.1V	70h	14.2V
08h	3.8V	1Dh	5.9V	32h	8V	47h	10.1V	5Ch	12.2V	71h	14.3V
09h	3.9V	1Eh	6V	33h	8.1V	48h	10.2V	5Dh	12.3V	72h	14.4V
0Ah	4V	1Fh	6.1V	34h	8.2V	49h	10.3V	5Eh	12.4V	73h	14.5V
0Bh	4.1V	20h	6.2V	35h	8.3V	4Ah	10.4V	5Fh	12.5V	74h	14.6V
0Ch	4.2V	21h	6.3V	36h	8.4V	4Bh	10.5V	60h	12.6V	75h	14.7V
0Dh	4.3V	22h	6.4V	37h	8.5V	4Ch	10.6V	61h	12.7V	76h	14.8V
0Eh	4.4V	23h	6.5V	38h	8.6V	4Dh	10.7V	62h	12.8V	77h	14.9V
0Fh	4.5V	24h	6.6V	39h	8.7V	4Eh	10.8V	63h	12.9V	78h	15V
10h	4.6V	25h	6.7V	3Ah	8.8V	4Fh	10.9V	64h	13V		
11h	4.7V	26h	6.8V	3Bh	8.9V	50h	11V	65h	13.1V		
12h	4.8V	27h	6.9V	3Ch	9V	51h	11.1V	66h	13.2V	Other	Reserved
13h	4.9V	28h	7V	3Dh	9.1V	52h	11.2V	67h	13.3V		
14h	5V	29h	7.1V	3Eh	9.2V	53h	11.3V	68h	13.4V		

VSNL[6:0]:

[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage
00h	-3V	15h	-5.1V	2Ah	-7.2V	3Fh	-9.3V	54h	-11.4V	69h	-13.5V
01h	-3.1V	16h	-5.2V	2Bh	-7.3V	40h	-9.4V	55h	-11.5V	6Ah	-13.6V
02h	-3.2V	17h	-5.3V	2Ch	-7.4V	41h	-9.5V	56h	-11.6V	6Bh	-13.7V
03h	-3.3V	18h	-5.4V	2Dh	-7.5V	42h	-9.6V	57h	-11.7V	6Ch	-13.8V
04h	-3.4V	19h	-5.5V	2Eh	-7.6V	43h	-9.7V	58h	-11.8V	6Dh	-13.9V
05h	-3.5V	1Ah	-5.6V	2Fh	-7.7V	44h	-9.8V	59h	-11.9V	6Eh	-14V
06h	-3.6V	1Bh	-5.7V	30h	-7.8V	45h	-9.9V	5Ah	-12V	6Fh	-14.1V
07h	-3.7V	1Ch	-5.8V	31h	-7.9V	46h	-10V	5Bh	-12.1V	70h	-14.2V
08h	-3.8V	1Dh	-5.9V	32h	-8V	47h	-10.1V	5Ch	-12.2V	71h	-14.3V
09h	-3.9V	1Eh	-6V	33h	-8.1V	48h	-10.2V	5Dh	-12.3V	72h	-14.4V
0Ah	-4V	1Fh	-6.1V	34h	-8.2V	49h	-10.3V	5Eh	-12.4V	73h	-14.5V
0Bh	-4.1V	20h	-6.2V	35h	-8.3V	4Ah	-10.4V	5Fh	-12.5V	74h	-14.6V
0Ch	-4.2V	21h	-6.3V	36h	-8.4V	4Bh	-10.5V	60h	-12.6V	75h	-14.7V
0Dh	-4.3V	22h	-6.4V	37h	-8.5V	4Ch	-10.6V	61h	-12.7V	76h	-14.8V
0Eh	-4.4V	23h	-6.5V	38h	-8.6V	4Dh	-10.7V	62h	-12.8V	77h	-14.9V
0Fh	-4.5V	24h	-6.6V	39h	-8.7V	4Eh	-10.8V	63h	-12.9V	78h	-15V
10h	-4.6V	25h	-6.7V	3Ah	-8.8V	4Fh	-10.9V	64h	-13V		
11h	-4.7V	26h	-6.8V	3Bh	-8.9V	50h	-11V	65h	-13.1V		
12h	-4.8V	27h	-6.9V	3Ch	-9V	51h	-11.1V	66h	-13.2V	Other	Reserved
13h	-4.9V	28h	-7V	3Dh	-9.1V	52h	-11.2V	67h	-13.3V		
14h	-5V	29h	-7.1V	3Eh	-9.2V	53h	-11.3V	68h	-13.4V		

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	02	0	0	0	0	0	0	1	0	POF	Power OFF Command Register
0	1		0	0	0	0	0	0	0	0		After power off command, driver will power off based on the Power OFF Sequence. BUSY_N will output low during operation. The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off. SD output will base on previous condition. *Remark: POF works at PON only
0	0	03	0	0	0	0	0	0	1	1	POFS	Power on/off Sequence Setting Register A[7:0] = 00h [POR]
0	1		0	0	A_5	A_4	0	0	A_1	A_0		A[5:4] ~ T_VDPG_OFF[1:0] Power off delay from VGH to VGL 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b: 80ms A[1:0] ~ T_VDS_OFF[1:0] Power off delay from VSHX/VSL to VGH 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b : 80ms
0	0	04	0	0	0	0	0	1	0	0	PON	Power ON Command Register After the Power ON command, driver will power on based on the Power ON Sequence. BUSY_N will output low during operation. * Remark: PON Include booster on, VSH1/VSH2/VSL regulator on With default BTST, timing is >80ms

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>06</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>BTST</td><td>VGH Booster Soft Start Setting Register (for VGH)
A[6:0] = 0Fh [POR]
B[6:0] = 04h [POR]
C[6:0] = 0Bh [POR]
D[6:0] = 10h [POR]
E[6:0] = 0Eh [POR]
F[6:0] = 10h [POR]
G[6:0] = 05h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td rowspan="8">A[3:2] ~ T_VGHSSA [1:0] = 11 (Default)
VGH booster soft start Phase A duration
A[1:0] ~ T_VGHSSB [1:0] = 11 (Default)
VGH booster soft start Phase B duration
<table><tr><th></th><th>Soft Start Phase Period (ms)</th></tr><tr><td>00</td><td>10</td></tr><tr><td>01</td><td>20</td></tr><tr><td>10</td><td>30</td></tr><tr><td>11</td><td>40</td></tr></table>
B[5:0] ~ VGHSSA_DRV [5:0] = 000100b (Default)
VGH Phase A Driving Strength
C[5:0] ~ VGHSSA_OFFT[[5:0] = 001011b (Default)
VGH Phase A Minimum OFF Time

D[5:0] ~ VGHSSB_DRV [5:0] = 010000b (Default)
VGH Phase B Driving Strength
E[5:0] ~ VGHSSB_OFFT[[5:0] = 001110b (Default)
VGH Phase B Minimum OFF Time

F[5:0] ~ VGHSSC_DRV [5:0] = 010000b (Default)
VGH Phase C Driving Strength
G[5:0] ~ VGHSSC_OFFT[[5:0] = 000101b (Default)
VGH Phase C Minimum OFF Time

Driving strength setting from strength1 to strength64 (strongest)

Minimum OFF Time (setting) from Period1 to Period64 (longest)</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>D_5</td><td>D_4</td><td>D_3</td><td>D_2</td><td>D_1</td><td>D_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>E_5</td><td>E_4</td><td>E_3</td><td>E_2</td><td>E_1</td><td>E_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>F_5</td><td>F_4</td><td>F_3</td><td>F_2</td><td>F_1</td><td>F_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>G_5</td><td>G_4</td><td>G_3</td><td>G_2</td><td>G_1</td><td>G_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>07</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>DSLP</td><td>Deep Sleep Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td></td><td>This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion.
The only one parameter is a check code, the command would be executed if check code is A5h.</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DTM</td><td>Data Start transmission Register</td></tr>
<tr><td colspan="10">2 bit per pixel</td><td rowspan="4">This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.

KPixel[1:0] Source Driver Output<table><tr><td></td><td>DDX=1 (Default)</td><td>DDX=0</td></tr><tr><td>00b</td><td>Gray 0</td><td>Gray 3</td></tr><tr><td>01b</td><td>Gray 1</td><td>Gray 2</td></tr><tr><td>10b</td><td>Gray 2</td><td>Gray 1</td></tr><tr><td>11b</td><td>Gray 3</td><td>Gray 0</td></tr></table>After issue this command, the host must send at least 1-byte data to the device.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>KPixel1 [1:0]</td><td></td><td>KPixel2 [1:0]</td><td></td><td>KPixel3 [1:0]</td><td></td><td>KPixel4 [1:0]</td><td></td></tr>
<tr><td>:</td><td></td><td></td><td colspan="8">…</td></tr>
<tr><td>0</td><td>1</td><td></td><td>KPixel (4M-3) [1:0]</td><td></td><td>KPixel (4M-2) [1:0]</td><td></td><td>KPixel (4M-1) [1:0]</td><td></td><td>KPixel (4M) [1:0]</td><td></td></tr>
<tr><td colspan="11"></td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>DRF</td><td>Display Refresh Command Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT.
BUSY_N will output low during operation.</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>17</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>AUTO</td><td>Auto Sequence Register</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>This command makes the chip enter the auto sequence
Single-chip application ONLY.
Auto Sequence Option
0xA5: Start Auto Sequence (PON > DRF > POF)
0xA7: Start Auto Sequence (PON > DRF > POF > DSLP).
Others: No effect
BUSY_N will output low during operation.</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>30</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PLL</td><td>Frame Rate Control register
The command controls the clock frequency.
A[3:0] = 2h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[3] ~ Dyna
Dynamic Frame Rate
0: Disable (Default)
1: Enable

A[2:0] ~ FR[2:0]
It supports the following frame rates.
Frame Rate Selection, Frame rate for Gate/Source switching that exclude the blanking time defined in CDI.<table><tr><td>FR[2:0]</td><td>Frame Rate Selection</td></tr><tr><td>000</td><td>12.5Hz</td></tr><tr><td>001</td><td>25Hz</td></tr><tr><td>010</td><td>50Hz (Default)</td></tr><tr><td>011</td><td>65Hz</td></tr><tr><td>100</td><td>75Hz</td></tr><tr><td>101</td><td>85Hz</td></tr><tr><td>110</td><td>100Hz</td></tr><tr><td>111</td><td>120Hz</td></tr></table></td></tr>
<tr><td colspan="12"></td></tr>
</table>

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	40	0	1	0	0	0	0	0	0	TSC	Temperature Sensor Command Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		This command enables internal temperature sensor. BUSY_N will output low during operation. Then the temperature value can be read in 1degC step A[7:0] ~ TS[7:0]

TS[7:0]:

A[7:0]	Value(°C)	A[7:0]	Value(°C)	A[7:0]	Value(°C)	A[7:0]	Value(°C)	A[7:0]	Value(°C)
E7h	-25	F7h	-9	07h	7	17h	23	27h	39
E8h	-24	F8h	-8	08h	8	18h	24	28h	40
E9h	-23	F9h	-7	09h	9	19h	25	29h	41
EAh	-22	FAh	-6	0Ah	10	1Ah	26	2Ah	42
EBh	-21	FBh	-5	0Bh	11	1Bh	27	2Bh	43
ECh	-20	FCh	-4	0Ch	12	1Ch	28	2Ch	44
EDh	-19	FDh	-3	0Dh	13	1Dh	29	2Dh	45
EEh	-18	FEh	-2	0Eh	14	1Eh	30	2Eh	46
EFh	-17	FFh	-1	0Fh	15	1Fh	31	2Fh	47
F0h	-16	00h	0	10h	16	20h	32	30h	48
F1h	-15	01h	1	11h	17	21h	33	31h	49
F2h	-14	02h	2	12h	18	22h	34	32h	50
F3h	-13	03h	3	13h	19	23h	35	Other	Reserved
F4h	-12	04h	4	14h	20	24h	36		
F5h	-11	05h	5	15h	21	25h	37		
F6h	-10	06h	6	16h	22	26h	38		

0	0	41	0	1	0	0	0	0	0	1	TSE	Temperature Sensor Enable Register This command selects Temperature offset A[7:0] = 00h [POR]
0	1		0	0	0	0	A_3	A_2	A_1	0		A[3:0] ~ TO[3:1] , Temperature offset:

TO[3:1]	Calculation	TO[3:1]	Calculation
000	+0	100	-4
001	+1	101	-3
010	+2	110	-2
011	+3	111	-1

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>50</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>CDI</td><td>VCOM and DATA interval setting Register
This command indicates the Border Output Selection and the interval between Vcom and data output
A[7:0] = 97h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>A[7:5]~VBD [2:0]
Border Output Selection:
<table>
<tr><td></td><td>DDX=1</td><td>DDX=0</td></tr>
<tr><td>VBD[2:0]</td><td>LUT (Default)</td><td>LUT</td></tr>
<tr><td>000</td><td>Gray 0</td><td>HIZ</td></tr>
<tr><td>001</td><td>Gray 1</td><td>Gray 3</td></tr>
<tr><td>010</td><td>Gray 2</td><td>Gray 2</td></tr>
<tr><td>011</td><td>Gray 3</td><td>Gray 1</td></tr>
<tr><td>100</td><td>HIZ(Default)</td><td>Gray 0</td></tr>
</table>
A[4]: DDX
Data Polarity for Pixel Data (See DTM command)
0: Invert
1: Non-invert (Default)
A[3:0] ~ CDI[3:0]
Gate and source blanking time (No gate source scanning)
<table>
<tr><td>CDI [3:0]</td><td>Interval (ms)</td><td>CDI [3:0]</td><td>Interval (ms)</td></tr>
<tr><td>0h</td><td>2</td><td>8h</td><td>40</td></tr>
<tr><td>1h</td><td>4</td><td>9h</td><td>60</td></tr>
<tr><td>2h</td><td>8</td><td>Ah</td><td>80</td></tr>
<tr><td>3h</td><td>12</td><td>Bh</td><td>100</td></tr>
<tr><td>4h</td><td>14</td><td>Ch</td><td>120</td></tr>
<tr><td>5h</td><td>16</td><td>Dh</td><td>140</td></tr>
<tr><td>6h</td><td>18</td><td>Eh</td><td>160</td></tr>
<tr><td>7h</td><td>20 (Default)</td><td>Fh</td><td>Reserved</td></tr>
</table>
User needs to review CDI setting to have stable VCOM in application</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>51</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>LPD</td><td>Lower Power Detection Register</td></tr>
<tr><td>1</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_0</td><td></td><td>BUSY_N will output low during operation.
Then the LPD status can be read.
A[0] ~ LPD status
0: Low power input
VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL
1: Normal (default)</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>60</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>TCON</td><td>TCON setting Register
This command defines non-overlap period of Gate and Source.
A[7:0] = 04h [POR]
B[7:0] = 02h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td rowspan="2">A[5:0] ~ S2G[5:0]
Source to Gate Non-overlap period
B[5:0] ~ G2S[5:0]
Gate to Source Non-overlap period
<table><tr><th>D[5:0]</th><th>S2G</th><th>G2S</th></tr><tr><td>00h</td><td>Reserved</td><td>3 unit</td></tr><tr><td>01h</td><td>Reserved</td><td>4 unit</td></tr><tr><td>02h</td><td>2 unit</td><td>5unit (Default)</td></tr><tr><td>03h</td><td>3 unit</td><td>6 unit</td></tr><tr><td>04h</td><td>4 unit (Default)</td><td>7 unit</td></tr><tr><td>05h</td><td>5 unit</td><td>8 unit</td></tr><tr><td>…</td><td>…</td><td>…</td></tr><tr><td>3Fh</td><td>63 unit</td><td>66 unit</td></tr></table>
Each time unit: ~0.5us

Remark:
Gate on time = line period – S2G – G2S
Min. Gate on time = 2unit
S2G + G2S ≤ line period – Min. Gate on time</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>61</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>TRES</td><td>Resolution setting Register
A[7:0] = B0h [POR]
B[8:0] = 128h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td rowspan="4">This command defines alternative resolution
A[7:0] ~ HRES[7:0]
Horizontal Display Resolution
Remark: Horizontal resolution should be 4-multiple.

B[8:0] ~ VRES[8:0]
Vertical Display Resolution
Remark: Vertical resolution should be 2-multiple.

e.g. HRES= B0h, VRES= 128h
<table><tr><th>UD,SHL</th><th>Source and gate sequence</th></tr><tr><td>00</td><td>S175,G295 to S0,G0</td></tr><tr><td>01</td><td>S0, G295 to S175,G0</td></tr><tr><td>10</td><td>S175,G0 to S0, G295</td></tr><tr><td>11</td><td>S0,G0 to S175, G295</td></tr></table>
Remark:
1) TRES is selected when PSR.RES=2’b00
2) VRES[8:0] >= 152</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td colspan="13"></td></tr>
</table>

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	62	0	1	1	0	0	0	1	0	HTOTAL	HTOTAL setting Register. This command defines line time for different frame rate. A[7:0] = 0x44 [POR], B[7:0] = 0x38 [POR]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Which defined the line time for HTOTAL_A to HTOTAL_B respectively. Frame time = HTOTAL timing x TRES.VRES[8:0] Timing of POR is matched for VRES = 296. Remark: 1) HTOTAL is effective when PSR.RES=2'b00 2) If user used TRES to define resolution, it needs to set the corresponding HTOTAL. Please refer to application note for details setting.
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	65	0	1	1	0	0	1	0	1	GSST	Gate/Source Start Setting Register. A[7:0] = 00h [POR] B[8:0] = 000h [POR]
0	1		0	0	0	0	0	0	0	0		A[7:0] ~ S_start[7:0] First valid source output channel setting S_start [7:0] / First valid source output 00h / S0 (Default) 04h / S4 08h / S8 … / … A8h / S168 ACh / S172 Other / Reserved B[8:0] ~ G_start[8:0] First valid gate output channel setting GSST and TRES can define the display window from target source and gate start and end line. Eg. GD: First G active = G16, G_start[8:0]=16. Last G active = G279, VRES[8:0]=264. SD: First S active = S8, S_start[7:0]=8. Last S active = S167, HRES[7:0]=160. Remark: 1) PSR.RES[1:0] = 00 (Map1) 2) G_start+VRES< 296, S_start+HRES< 176.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	70	0	1	1	1	0	0	0	0	REV	Chip Revision Register The command is to read the ID A[7:0] = C3 [POR] B[7:0] = 01h [POR] C[7:0] = 01h [POR]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	80	1	0	0	0	0	0	0	0	AMV	Auto Measurement VCOM Register This command implements related VCOM sensing setting. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	0	A_0		A[7:6] ~ P[1:0] Number of sensing Points 00: 2 (Default) 01: 4 10: 8 11: 16 A[5:4] ~AMVT[1:0] Auto Measure Vcom Time: Sensing Time 00: 5 sec. (Default) 01: 10 sec. 10: 15 sec. 11: 20 sec. A[3] ~ AMVX VCOM measurement Gate settings 0: Gate scan normally during VCOM measurement (Default) 1: All Gates ON during VCOM measurement A[2] ~ AMVS Source output of AMV: 0: Set Source output to 0V during Auto Measure VCOM period. (Default) 1: Set Source output to VSH_LV during Auto Measure VCOM period. A[0] ~ AMVE Auto Measure Vcom Enable (/Disable): 0: Disabled (Default) 1: Enabled BUSY_N will output low during operation. Note: AMV works at PON only

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	81	1	0	0	0	0	0	0	1	VV	Auto Measurement VCOM Register This command gets the Vcom value after AMV.
1	1		1	A_6	A_5	A_4	A_3	A_2	0	0		A[6:0] ~ VV[6:0]: Vcom read Value , valid range from -0.2V to -4.0V.

VV[6:0]:

A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage
04h	-0.2V	18h	-1.2V	2Ch	-2.2V	40h	-3.2V
06h	-0.3V	1Ah	-1.3V	2Eh	-2.3V	42h	-3.3V
08h	-0.4V	1Ch	-1.4V	30h	-2.4V	44h	-3.4V
0Ah	-0.5V	1Eh	-1.5V	32h	-2.5V	46h	-3.5V
0Ch	-0.6V	20h	-1.6V	34h	-2.6V	48h	-3.6V
0Eh	-0.7V	22h	-1.7V	36h	-2.7V	4Ah	-3.7V
10h	-0.8V	24h	-1.8V	38h	-2.8V	4Ch	-3.8V
12h	-0.9V	26h	-1.9V	3Ah	-2.9V	4Eh	-3.9V
14h	-1V	28h	-2V	3Ch	-3V	50h	-4V
16h	-1.1V	2Ah	-2.1V	3Eh	-3.1V	Other	Reserved

0	0	82	1	0	0	0	0	0	1	0	VDCS	VCM_DC Setting Register This command sets VCOM_DC value. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	0		A[7] ~ MTP _VCM Vcom follow VDCS after RESET. 0: Disable (Default), auto load from MTP if it is valid. 1: Enable, VCOM value from the VDCS[6:0] A[6:0] ~ VDCS[6:0]: VCOM_DC Setting, 0.1V step from -0.2V to -4V.

VDCS[6:0]:

A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage
04h	-0.2V	18h	-1.2V	2Ch	-2.2V	40h	-3.2V
06h	-0.3V	1Ah	-1.3V	2Eh	-2.3V	42h	-3.3V
08h	-0.4V	1Ch	-1.4V	30h	-2.4V	44h	-3.4V
0Ah	-0.5V	1Eh	-1.5V	32h	-2.5V	46h	-3.5V
0Ch	-0.6V	20h	-1.6V	34h	-2.6V	48h	-3.6V
0Eh	-0.7V	22h	-1.7V	36h	-2.7V	4Ah	-3.7V
10h	-0.8V	24h	-1.8V	38h	-2.8V	4Ch	-3.8V
12h	-0.9V	26h	-1.9V	3Ah	-2.9V	4Eh	-3.9V
14h	-1V	28h	-2V	3Ch	-3V	50h	-4V
16h	-1.1V	2Ah	-2.1V	3Eh	-3.1V	Other	Reserved

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>83</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>PTLW</td><td>PARTIAL WINDOW
This command sets partial window address.
A[7:0] = 00h [POR]
B[7:0] = AFh [POR]
C[8:0] = 000h [POR]
D[8:0] = 127h [POR]
E[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td rowspan="10">A[7:0] ~ HRST [7:0]
Horizontal start address
B[7:0] ~ HRED [7:0]
Horizontal end address
C[8:0] ~ VRST [8:0]
Vertical start address
D[8:0] ~ VRED [8:0]
Vertical end address

E[0] ~ PMODE
0: disable partial mode (Default)
1: enable partial mode
Gate scan both inside and outside of the partial window

Valid range
<table><tr><th></th><th>Conventional</th></tr><tr><td>HRST</td><td>0(000h) to 172(ACh) /step 4</td></tr><tr><td>HRED</td><td>3(003h) to 175(AFh) /step 4</td></tr><tr><td>VRST</td><td>0(000h) to 295(127h) /step 1</td></tr><tr><td>VRED</td><td>0(000h) to 295(127h) /step 1</td></tr></table>
Requirement:
1) HRST [8:0]<= HRED [8:0]
2) VRST [8:0]<= VRED [8:0]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C8</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td><td>C0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D8</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>E0</td><td></td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>90</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PGM</td><td>Program Mode
This command is to set MTP program mode
After this command is issued, the chip would enter the program mode.
After the programming procedure completed, a hardware reset is necessary for leave the program mode
BUSY_N will output low until PGM mode is ready.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>91</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>APG</td><td>Active Program
This command is to execute MTP program
After this command is issued, the chip would program the MTP.
BUSY_N will output low during operation.
Requirement: In PON mode with internal programming power.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>92</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">RMTP</td><td>Read MTP Data</td></tr>
<tr><td>1</td><td>1</td><td></td><td colspan="8">1st ~ dummy
2nd ~ N+1th Parameter</td><td>This command is to read the MTP content from SRAM.
The 1st byte read is dummy byte.
The 2nd byte read is the content of Address 0 in MTP
The N+1th byte read is the content of Address n in MTP
After issue this command, the host must read at least 1 byte data from the device.</td></tr>
<tr><td colspan="13"></td></tr>
</table>

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	93	1	0	0	1	0	0	1	1	RSRAM	Read SRAM Data This command is to read the content from SRAM. The 1st byte read is dummy byte. The 2nd byte read is the content of Address 0 in SRAM. The N+1th byte read is the content of Address n in SRAM. After issue this command, the host must read at least 1 byte data from the device.
1	1		1st ~ dummy 2nd ~ N+1th Parameter									
0	0	A2	1	0	1	0	0	0	1	0	PGM_CFG	MTP Program Config This command is to set the configuration of MTP
0	1		0	0	1	1	0	A_2	A_1	A_0		A[2:0] ~ PGM_UMODE[2:0] 000b: Reserved 001b: Compressed LUT (Default) 010b: Init Code Others: Reserved B[7:0] ~ PGM_SADDR[15:8], C[7:0] ~ PGM_SADDR[7:0] Program Start Address: Compressed LUT: 0000h D[7:0] ~ PGM_DSIZE [15:8] E[7:0] ~ PGM_DSIZE [7:0] Program data size in bytes
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	0	A3	1	0	1	0	0	0	1	1	PGM_STAT	MTP Program Status This command is to read MTP Program status A[7:0] = 00h [POR]
1	1		0	0	0	0	0	0	A_1	A_0		A[1] ~ PGM_VER_ERR Data verification of APG 0: OK 1: NOK A[0] ~ PGM_EXE_ERR MTP program execution status 0: Normal 1: Invalid APG setting
0	0	A4	1	0	1	0	0	1	0	0	MTP_STAT	MTP Status Register This command is to read MTP status A[7:0] = 00h [POR] B[7:0] = 00h [POR] C[7:0] = 00h [POR]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7] ~ LUT_TYPE[7] User MTP Type 0: Blank 1: Compressed A[6:0] ~ Reserved B[7:0] ~ Reserved C[7:0] ~ FREE_UI[7:0] Next Free Space Address for User Init Code
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

<table>
<tr><th>R/W#</th><th>DC</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>E0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>CCSET</td><td>CCSET for temperature input selection
A[7:0] = 00h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_1</td><td>0</td><td></td><td>A[1] = TSFIX
Temperature Input selection
0: Use Internal Temperature sensor (Default)
1: Use TSSET[7:0] value</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>E3</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>PWS</td><td>Power Saving Register
This command is sets for saving power VCOM/Source power saving during display refresh period.
A[7:0] = 65h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td>If the output voltage of VCOM/Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

A[7:4] = VCOM_W [3:0]
<table>
<tr><th>VCOM_W [3:0]</th><th>VCOM_power saving width. (time unit)</th><th>VCOM_W [3:0]</th><th>VCOM_power saving width. (time unit)</th></tr>
<tr><td>0</td><td>Reserved</td><td>8</td><td>8</td></tr>
<tr><td>1</td><td>1</td><td>9</td><td>9</td></tr>
<tr><td>2</td><td>2</td><td>10</td><td>10</td></tr>
<tr><td>3</td><td>3</td><td>11</td><td>11</td></tr>
<tr><td>4</td><td>4</td><td>12</td><td>12</td></tr>
<tr><td>5</td><td>5</td><td>13</td><td>13</td></tr>
<tr><td>6</td><td>6[Default]</td><td>14</td><td>14</td></tr>
<tr><td>7</td><td>7</td><td>15</td><td>15</td></tr>
</table>
A[3:0] = SD_W [3:0]
<table>
<tr><th>SD_W [3:0]</th><th>Source power saving width[us]</th><th>SD_W [3:0]</th><th>Source power saving width [us]</th></tr>
<tr><td>0</td><td>Reserved</td><td>8</td><td>4</td></tr>
<tr><td>1</td><td>0.5</td><td>9</td><td>4.5</td></tr>
<tr><td>2</td><td>1</td><td>10</td><td>5</td></tr>
<tr><td>3</td><td>1.5</td><td>11</td><td>5.5</td></tr>
<tr><td>4</td><td>2</td><td>12</td><td>6</td></tr>
<tr><td>5</td><td>2.5[Default]</td><td>13</td><td>6.5</td></tr>
<tr><td>6</td><td>3</td><td>14</td><td>7</td></tr>
<tr><td>7</td><td>3.5</td><td>15</td><td>7.5</td></tr>
</table>
*Remark:
VCOM_W setting < CDI setting
SD_W setting < S2G setting</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>E4</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>LVSEL</td><td>LVD Voltage Select Register
This command is sets for low power detect level power
A[1:0] = 3h [POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td></td><td>A[1:0] ~ LVD_SEL[1:0]
Low power detection threshold
00: 2.2V
01: 2.3V
10: 2.4V
11 : 2.5V (Default)</td></tr>
</table>

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	E6	1	1	1	0	0	1	1	0	TSSET	Manual input temperature value This command is to force the TS value A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:0] ~ TS_SET[7:0] When TSFIX=1, Temperature value will be set by TS_SET[7:0]. Format of the temperature value is 8-bit binary value and it is 1degC per step.

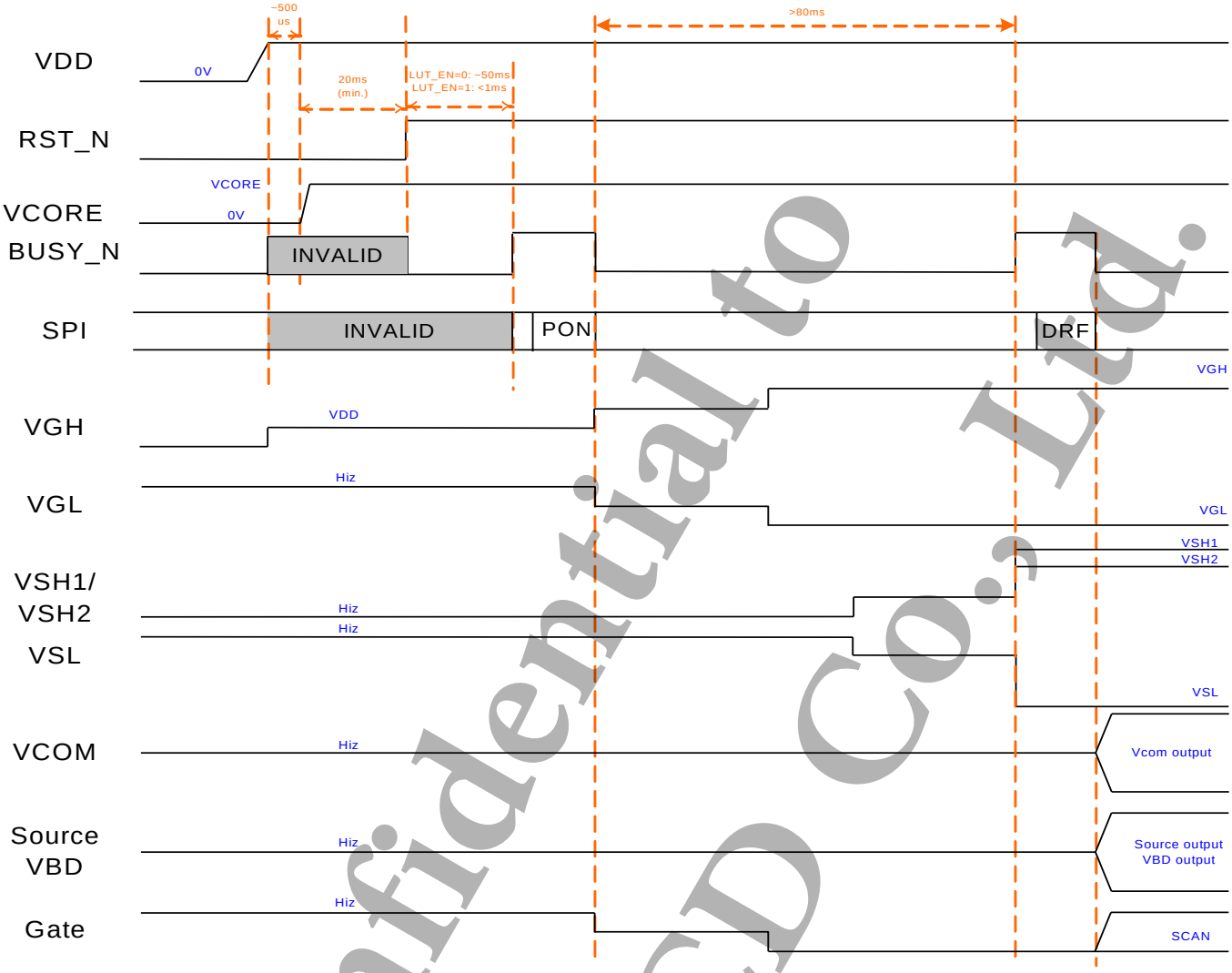
TS_SET[7:0]:

A[7:0]	Value(degC)	A[7:0]	Value(degC)	A[7:0]	Value(degC)
E7h	-25	01h	1	1Bh	27
E8h	-24	02h	2	1Ch	28
E9h	-23	03h	3	1Dh	29
EAh	-22	04h	4	1Eh	30
EBh	-21	05h	5	1Fh	31
ECh	-20	06h	6	20h	32
EDh	-19	07h	7	21h	33
EEh	-18	08h	8	22h	34
EFh	-17	09h	9	23h	35
F0h	-16	0Ah	10	24h	36
F1h	-15	0Bh	11	25h	37
F2h	-14	0Ch	12	26h	38
F3h	-13	0Dh	13	27h	39
F4h	-12	0Eh	14	28h	40
F5h	-11	0Fh	15	29h	41
F6h	-10	10h	16	2Ah	42
F7h	-9	11h	17	2Bh	43
F8h	-8	12h	18	2Ch	44
F9h	-7	13h	19	2Dh	45
FAh	-6	14h	20	2Eh	46
FBh	-5	15h	21	2Fh	47
FCh	-4	16h	22	30h	48
FDh	-3	17h	23	31h	49
FEh	-2	18h	24	32h	50
FFh	-1	19h	25	Other	Reserved
00h	0	1Ah	26		

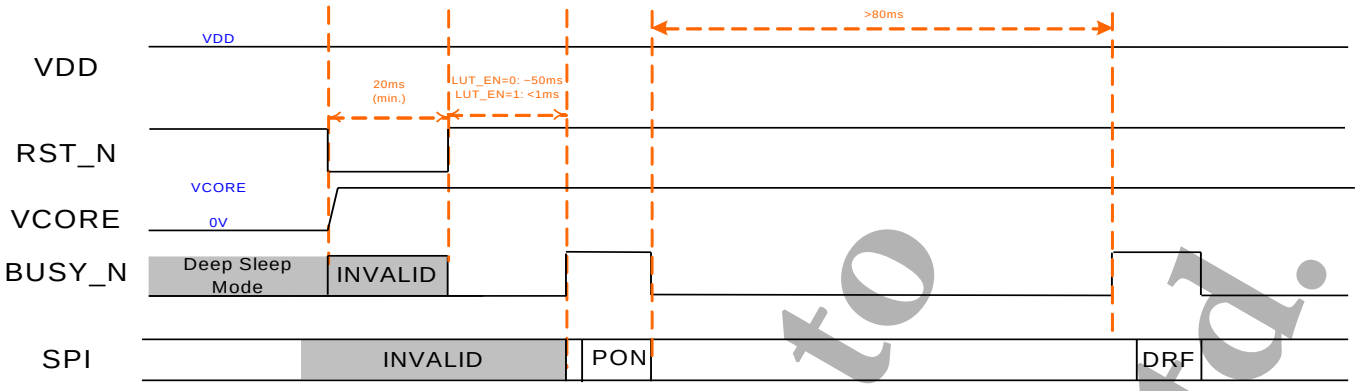
0	0	E7	1	1	1	0	0	1	1	1	PST	VGH Booster Soft Start Setting Register (for VGH) during switch mode A[5:0] = 10h [POR] B[5:0] = 05h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[5:0] ~ VGHSM_DRV [5:0] = 010000b (Default) VGH switch mode Driving Strength
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		B[5:0] ~ VGHSM_OFFT[[5:0] = 000101b (Default) VGH switch mode Minimum OFF Time Remark: PSR.B_mode=1

9 Display on/off Sequence

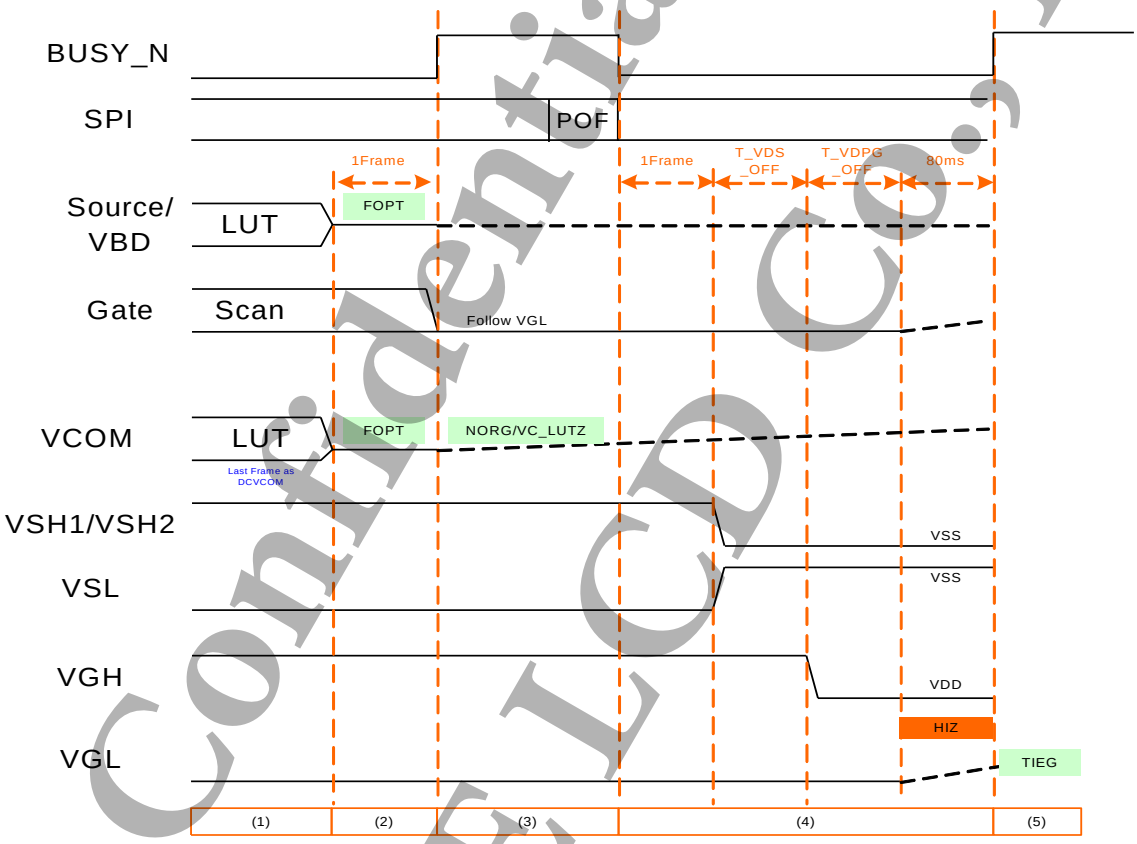
9.1 Display on sequence from VDD power on



9.2 Display on sequence from deep sleep mode



9.3 Display off Sequence Display



Note: If VCOM and VGL set as floating after display update. Please wait until the system completely discharge before next operation.

10 Absolute Maximum Rating

Table 10-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-30 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VDD be constrained to the range GND < VDD. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either GND or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 Electrical Characteristics

The following specifications apply for: GND=0V, VDD=3.0V, T_{OPR}=25ºC.

Table 11-1: DC Characteristics

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	VDD supply operation voltage	VDD		2.2	3.0	3.6	V
V_{COM_DC}	VCOM_DC output voltage	VCOM		-4.0	-	-0.2	V
dV_{COM_DC}	VCOM_DC output voltage deviation	VCOM	No output load	-200	-	200	mV
V_{COM_AC}	VCOM_AC output voltage	VCOM		V_{SL} + V_{COM_DC}	V_{COM_DC}	V_{SH} + V_{COM_DC}	V
V_{GATE}	Gate output voltage	G0~G295		-20	-	+20	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage	G0~G295		-	-	40	V
VSH	Positive Source output voltage	VSH1		+3		+15	V
VSH2	Positive Source output voltage	VSH2		+3		+15	V
dV_{SH}	VSH1/VSH2 output voltage deviation	VSH1/ VSH2	No output load	-200	-	200	mV
V_{SL}	Negative Source output voltage	VSL		-15		-3	V
dV_{SL}	VSL output voltage deviation	VSL	No output load	-200	-	200	mV
V_{IH}	High level input voltage	SDA SCL, CSB, D/C, RST_N, BS1, M/S#		0.8V_{DDIO}	-	-	V
V_{IL}	Low level input voltage			-	-	0.2V_{DDIO}	V
V_{OH}	High level output voltage	SDA, BUSY_N,	IOH = -100uA	0.8V_{DDIO}	-	-	V
V_{OL}	Low level output voltage		IOL = 100uA	-	-	0.2V_{DDIO}	V

Symbol	Parameter	Applicable pin	Test Condition	Min.	Typ.	Max.	Unit
Idslp_VDD	deep sleep current	VDD	- DC/DC off - No clock - No output load - No MCU interface access - Cannot retain RAM data			1	uA
Iopr_VDD	Operating Mode current	VDD	VDD=3V		1		mA
V_{GH}	Operating Mode Output Voltage	VGH	After PON Command VGH=20V VGL=-VGH VSH=15V VSH2=15V VSL=-15V VCOM = -2V No waveform transitions. No output load No RAM read/write	19.5	20	20.5	V
V_{SH}		VSH1		14.8	15	15.2	V
V_{SH2}		VSH2		14.8	15	15.2	V
V_{SL}		VSL		-15.2	-15	-14.8	V
V_{COM}		VCOM		-2.2	-2	-1.8	V

12 AC Characteristics

12.1 Serial Peripheral Interface

The following specifications apply for: VDDIO - GND = 2.3V to 3.6V, T_{OPR} = 25°C, CL=20pF

Table 12-1: Serial Peripheral Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB select setup time	60			ns
t_{SCH}	CSB select hold time	65			ns
t_{SCC}	CSB deselect setup time	25			ns
t_{CHW}	CSB deselect hold time	100			ns
t_{SCYCW}	Serial clock cycle (Write)	50			ns
t_{SHW}	SCL “H” pulse width (Write)	25			ns
t_{SLW}	SCL “L” pulse width (Write)	25			ns
t_{SCYCL}	Serial clock cycle (Read)	400			ns
t_{SHR}	SCL “H” pulse width (Read)	180			ns
t_{SLR}	SCL “L” pulse width (Read)	180			ns
t_{SDS}	Data setup time	30			ns
t_{SDH}	Data hold time	30			ns
t_{DCS}	DC setup time	40			ns
t_{DCH}	DC hold time	40			ns
t_{ACC}	Access time			100	ns
t_{OH}	Output disable time	15			ns

Note: All timings are based on 20% to 80% of VDDIO-GND

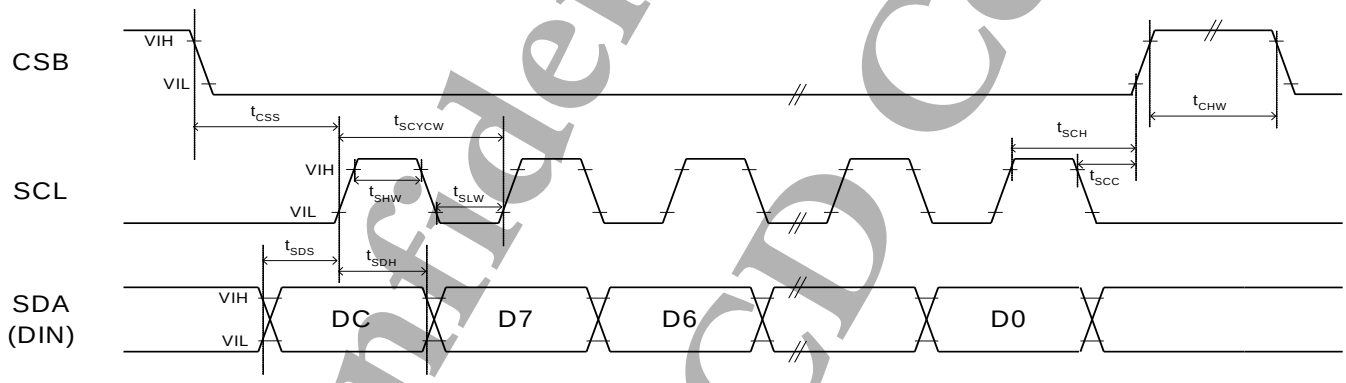


Figure 12-1: 3-wire SPI characteristics (write mode)

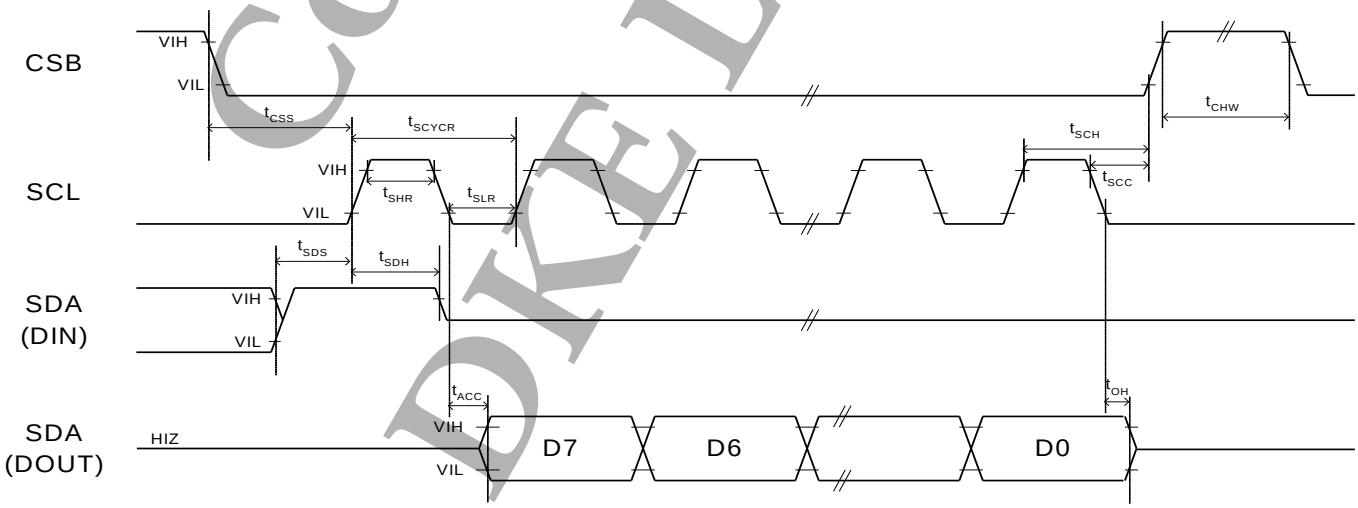


Figure 12-2: 3-wire SPI characteristics (read mode)

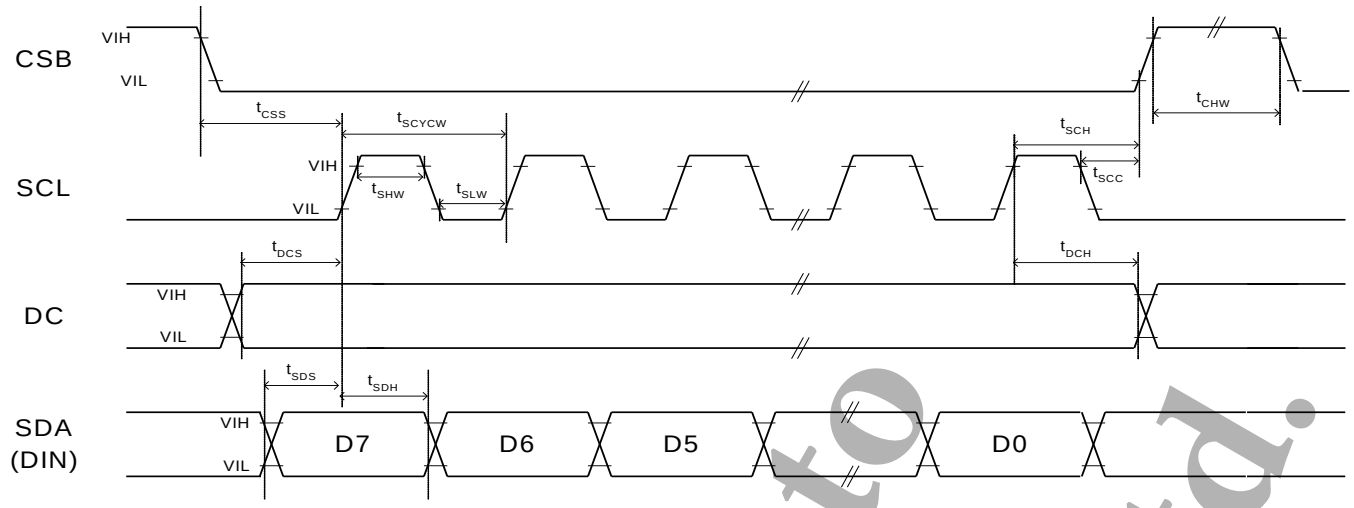


Figure 12-3: 4-wire SPI characteristics (write mode)

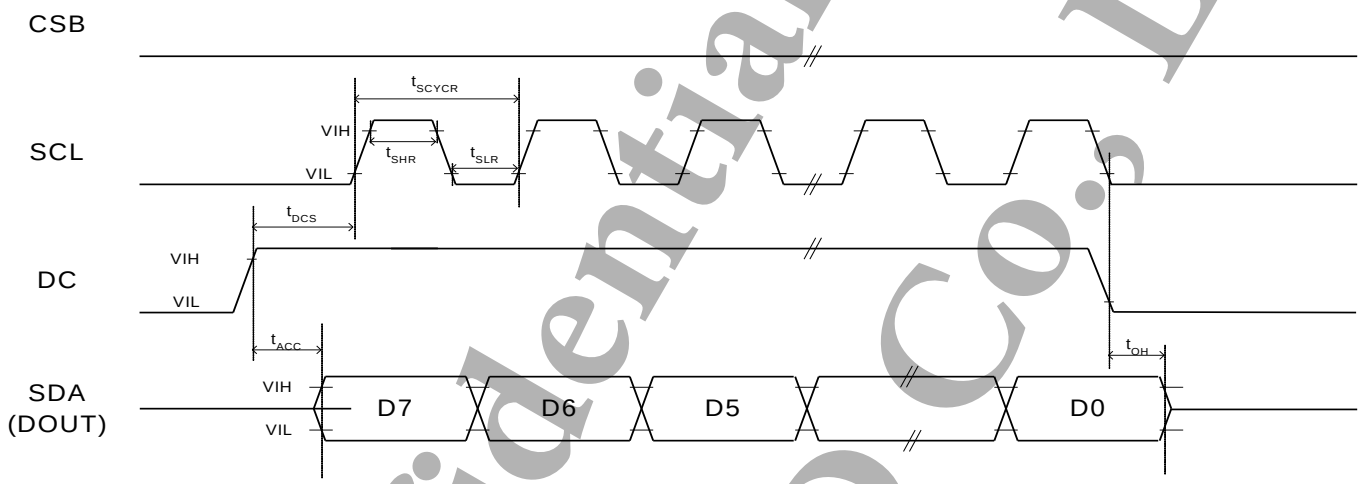


Figure 12-4: 4-wire SPI characteristics (read mode)

13 Application Circuit

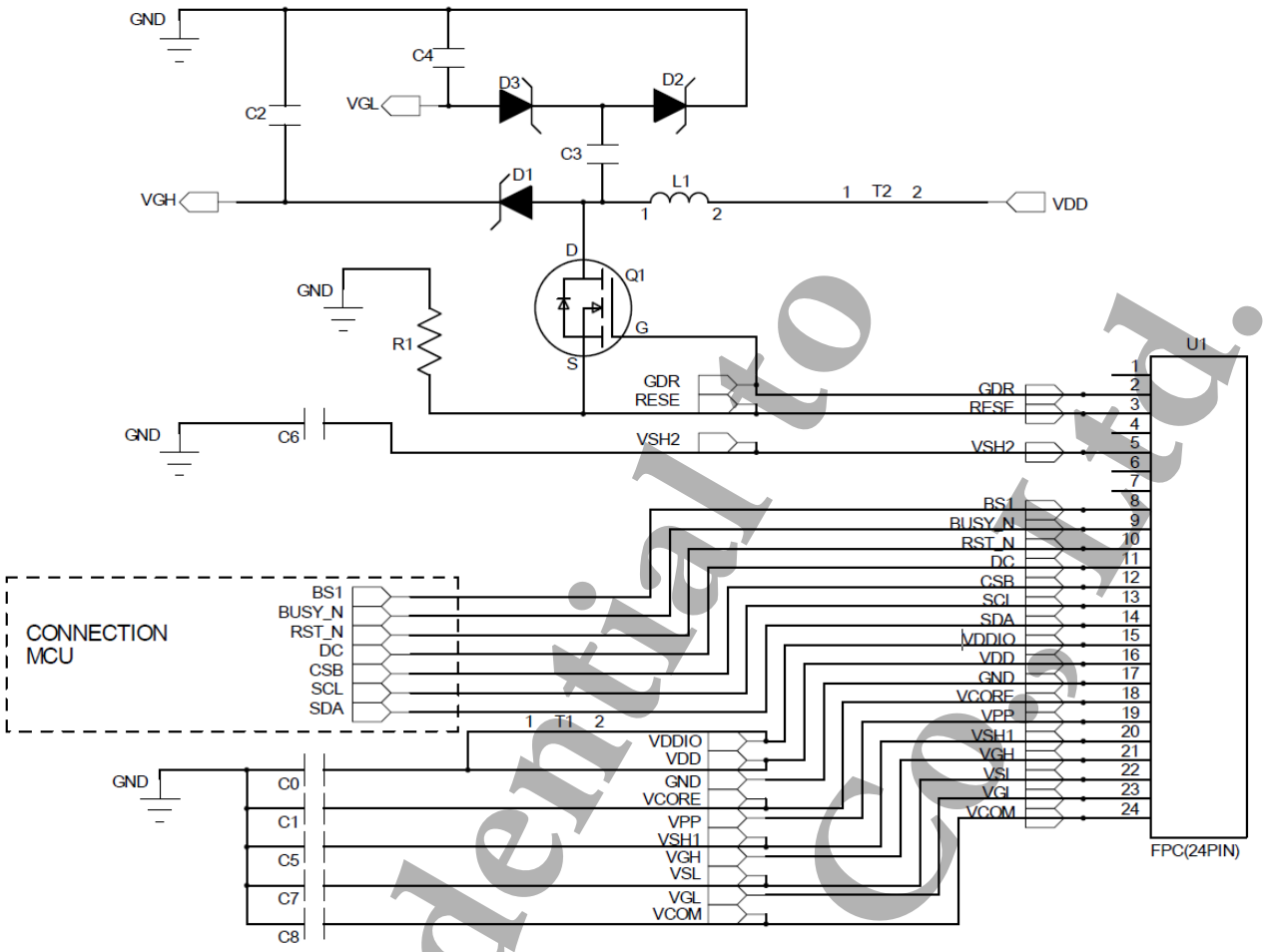


Figure 13-1: SSD2680A application circuit

Table 13-1: Component list for SSD2680A application circuit

Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	0.47uF, 1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
R1	2.2 ohm	0402/0603/0805; 1% variation, ≥ 0.05W
D1-D3	Diode	MBR0530 1) Reverse DC voltage ≥ 30V 2) Io ≥ 500mA 3) Forward voltage ≤ 430mV
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage ≥ 30V 2) Vgs(th) = 0.9V (Typ), 1.3V (Max) 3) Rds on ≤ 2.1Ω @ Vgs = 2.5V
L1	47uH	CDRH2D18 / LDNP-470NC Io= 500mA (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

Remarks:

1) The recommended component value and reference part in Table 13-1 is subject to change depending on panel loading.
2) Customer is required to review if the selected component value and part is suitable for their application.

14 Package Information

TBD

The product(s) listed in this datasheet comply with Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances and People’s Republic of China Electronic Industry Standard GB/T 26572-2011 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)”. Hazardous Substances test report is available upon request.

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