2.13 inch
E-paper Display Series

GooDisplay®

GDEY0213F61H

Dalian Good Display Co., Ltd.

Product Specifications

Customer	Standard
Description	ePaper Display
Model Name	GDEY0213F61H
Date	2025/10/26
Revision	1.0

	Design Engineering		
	Approval	Check	Design
			

Zhongnan Building, No.18, Zhonghua West ST,Ganjingzi DST,Dalian,CHINA
Tel: +86-411-84619565
Email: info@good-display.com
Website: www.good-display.com

CONTENTS

1. Overview

GDEY0213F61H is a reflective electrophoretic technology display module on an active matrix TFT substrate. The panel is capable of displaying black, white, yellow, and red images depending on the associated lookup table used. The circuitry on the panel includes an integrated gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memory to store the frame buffer and lookup tables, along with additional circuitry to control VCOM and BORDER settings.

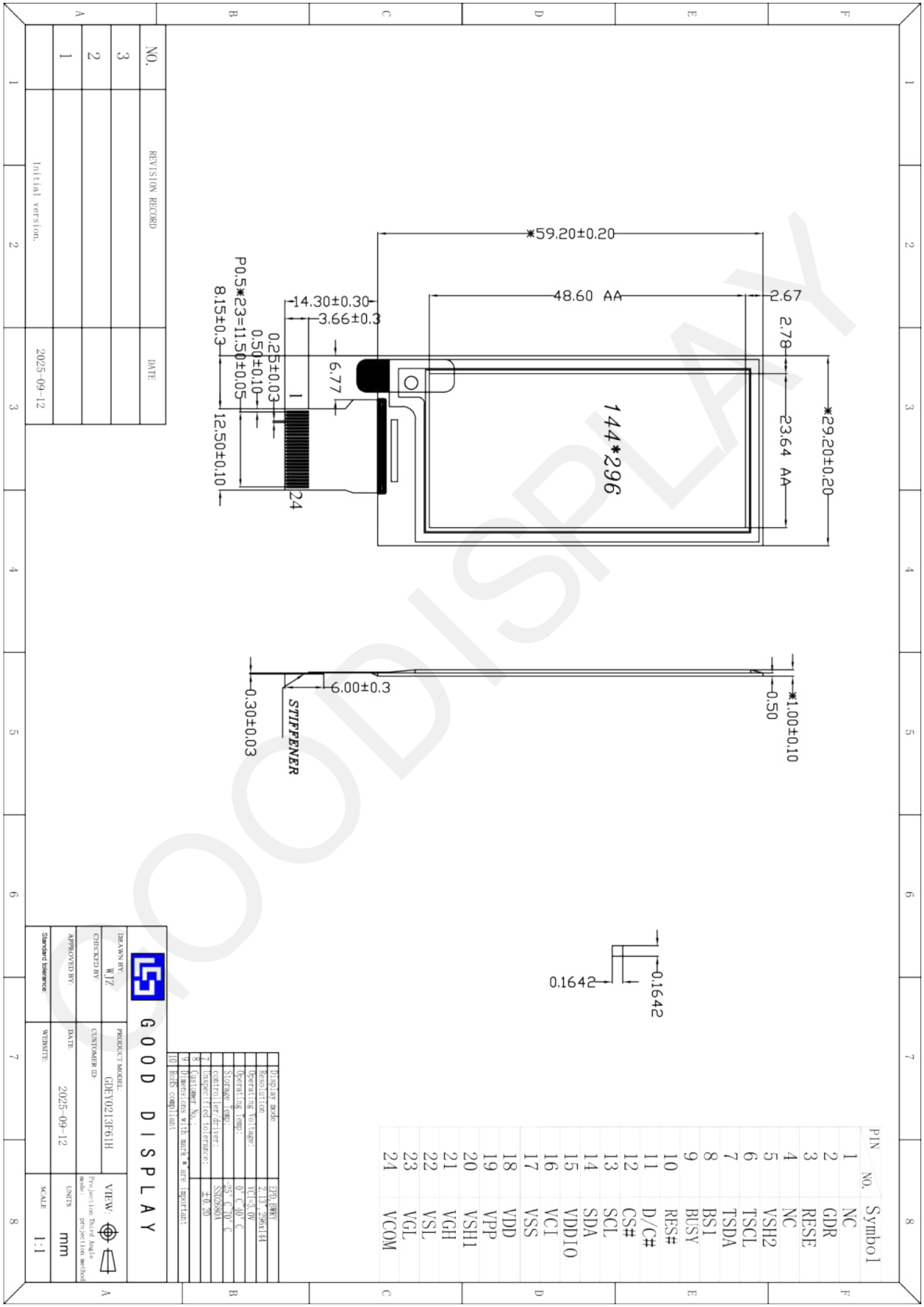
2. Features

Highlight Red and Yellow color
High contrast
High reflectance
Ultra wide viewing angle
Ultra low power consumption
Pure reflective mode
Bi-stable display
Antiglare hard-coated front-surface
Low current deep sleep mode
On chip display RAM
Waveform stored in On-chip OTP
Serial peripheral interface available
On-chip oscillator
On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
I²C signal master interface to read external temperature sensor
Available in COG package

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	144 (H)×296 (V)	Pixel	Dpi:154
Active Area	23.64×48.60	mm	
Pixel Pitch	0.1642×0.1642	mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.2(H)×59.2(V)×1.0(D)	mm	
Weight	3.3±0.5	g	

4. Mechanical Drawing of EPD module



5. Input/Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	This pin is N-MOS gate control.	
3	RESE	I	Current sense input for control loop.	
4	NC		Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage	
6	NC		Do not connect with other NC pins	Keep Open
7	NC		Do not connect with other NC pins	Keep Open
8	BS1	I	Interface Selection Pin	
9	BUSY	O	This pin indicates the driver status	
10	RES#	I	This pin is reset signal input.Active Low.	
11	D/C#	I	This pin is Data/Command control pin connecting to the MCU.	
12	CS#	I	This pin is the chip select input connecting to the MCU.	
13	SCL	I	Serial clock pin for interface	
14	SDA	I/O	Serial data pin for interface	
15	VDDIO	P	Power for interface logic pins	
16	VCI	P	Power Supply pin for the chip	
17	VSS	P	Ground	
18	VDD	P	Core logic power pin	
19	VPP	P	Reserved.	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

Note:I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to GND, Pull H = connect to VDDIO

6. Electrical Characteristics

6.1 Absolute Maximum Rating

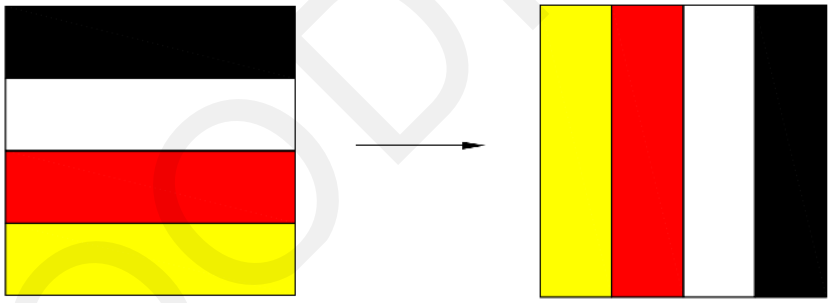
Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VDDIO+0.5	V
Logic Output voltage	VOUT	-0.5to VDDIO+0.5	
Operating Temp range	TOPR	0 to +40	ºC
Storage Temp range	TSTG	-25to +70	ºC
Optimal Storage Temp	TSTGo	23±2	ºC
Optimal Storage Humidity	HSTGo	55±10	%RH

Note: Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits provided in the Electrical Characteristics tables or the Pin Description section.

6.2 Panel DC Characteristics

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.2	3.0	3.6	V
High level input voltage	V_{IH}	-	-	$0.8V_{DDIO}$	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	$0.2V_{DDIO}$	V
High level output voltage	V_{OH}	IOH = -100uA	-	$0.8V_{DDIO}$	-	-	V
Low level output voltage	V_{OL}	IOL =100uA	-	-	-	$0.2V_{DDIO}$	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	9	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_V_{CI}	V_{CI} =3.0V	-	-	3	-	mA
Fast/Full Image update	-	25 ºC	-	-	12/16	-	sec
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No output load No MCU interface access Cannot retain RAM data	-	-	1	-	uA

Notes: 1. The typical power is measured with following transition from horizontal 4 scale pattern tovertical 4 scale pattern.



2. The deep sleep power is the power consumed when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are guaranteed only when using the controller and waveform provided by GOODISPLAY.

4. Electrical measurement method: Multimeter.

6.3 AC Characteristics

6.3.1 MCU Interface Selection

The IC supports both 3-wire and 4-wire serial peripheral interfaces. On the IC, the MCU interface is pin-selectable via the BS1 pin, as detailed in Table 6-1.

Table 6-1: Interface pins assignment under different MCU interface

MCU Interface	BS1	RST_N	CSB	DC	SCL	SDA
4-wire serial peripheral interface (SPI)	L	Required	CSB	DC	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	CSB	L	SCL	SDA

Note

(1) L is connected to GND and H is connected to VDDIO

6.3.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, DC and CSB. The control pins status in 4-wireSPIin reading/writing command/data is shown in Table 6-2. The read/write procedure of 4-wire SPIis shown inFigure 6-1.

Table 6-2: Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	L	L
Read/Write data	↑	Data bit	H	L

Note:

(1) L is connected to GND and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

(3) SDA (Write Mode) is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C pin.

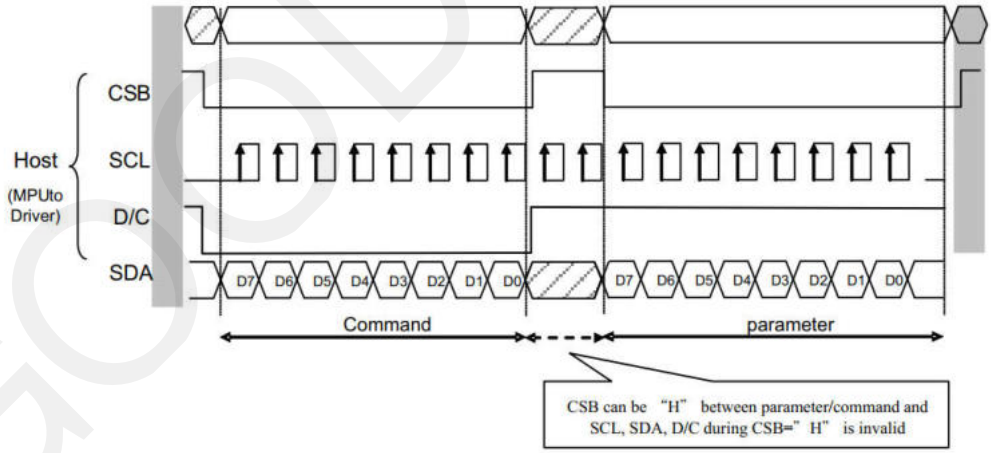


Figure 6-1: Read/Write procedure in 4-wire SPl mode

6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire SPI consists of a serial clock (SCL), serial data (SDA), and CSB. Its operation is similar to the 4-wire SPI, but the DC pin is not used and must be tied to LOW. The control pin status for the 3-wire SPI is shown in Table 6-3.

During read/write operations, 9-bit data is shifted into the shift register on every rising clock edge. The bit-shifting sequence is: DC bit, D7 bit, D6 bit, down to D0 bit. The first bit is the DC bit, which determines whether the following byte is a command or data. When the DC bit is 0, the following byte is a command. When the DC bit is 1, the following byte is data. The read/write procedure for the 3-wire SPI is shown in Figure 6-2.

Table 6-3: Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	DC pin	CSB pin
Write command	↑	Command bit	Tie LOW	L
Read/Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to GND and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

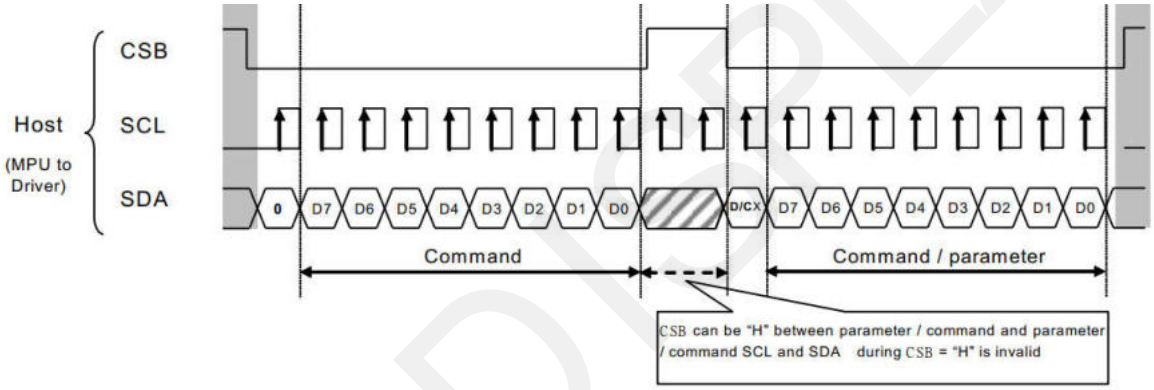
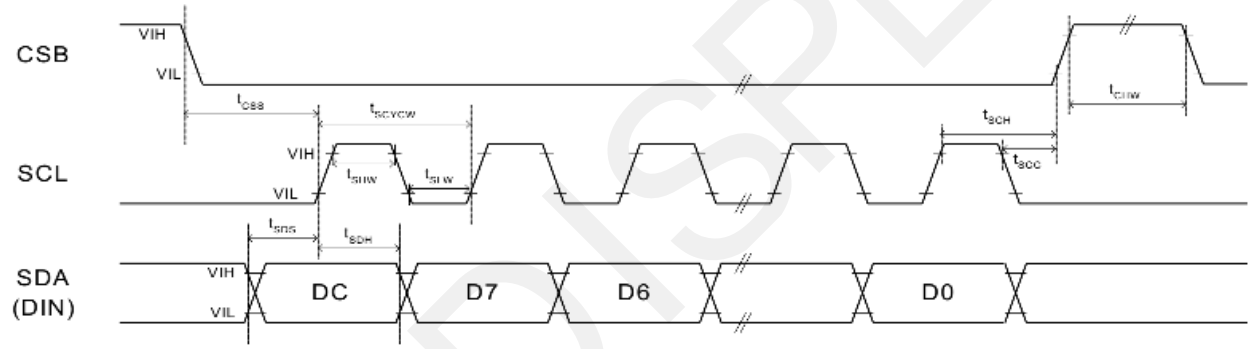


Figure 6-2:Read/Write procedure in 3-wire SPI mode

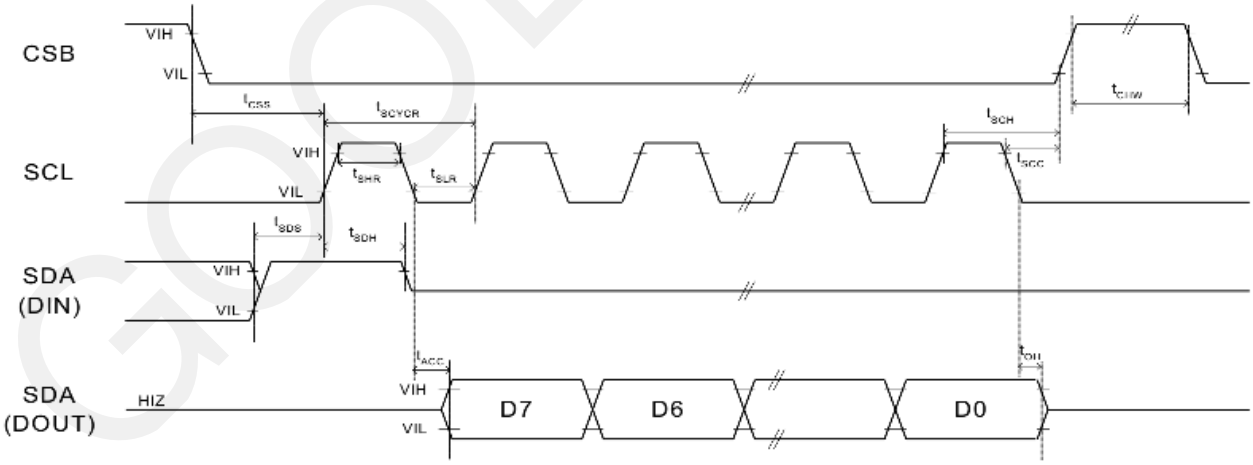
6.3.4 Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{CSS}	CSB select setup time	60			ns
t_{SCH}	CSB select hold time	65			ns
t_{SCC}	CSB deselect setup time	25			ns
t_{CHW}	CSB deselect hold time	100			ns
t_{SCYCW}	Serial clock cycle (Write)	50			ns
t_{SHW}	SCL "H" pulse width (Write)	25			ns
t_{SLW}	SCL "L" pulse width (Write)	25			ns
t_{SCYCL}	Serial clock cycle (Read)	400			ns
t_{SHR}	SCL "H" pulse width (Read)	180			ns
t_{SLR}	SCL "L" pulse width (Read)	180			ns
t_{SDS}	Data setup time	30			ns
t_{SDH}	Data hold time	30			ns
t_{DCS}	DC setup time	40			ns
t_{DCH}	DC hold time	40			ns
t_{ACC}	Access time			100	ns
t_{OH}	Output disable time	tbd			ns

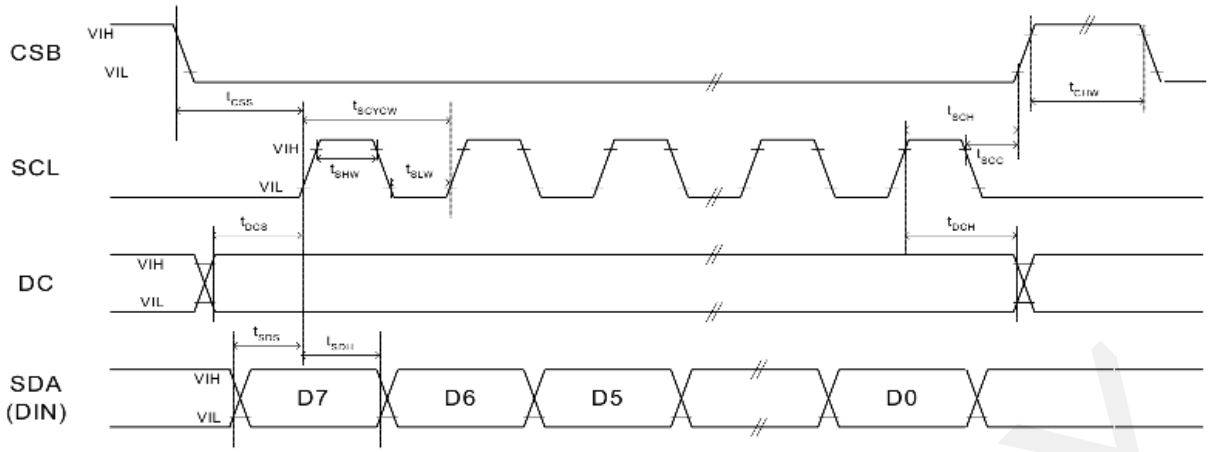
Note: All timings are based on 20% to 80% of VDDIO-GND



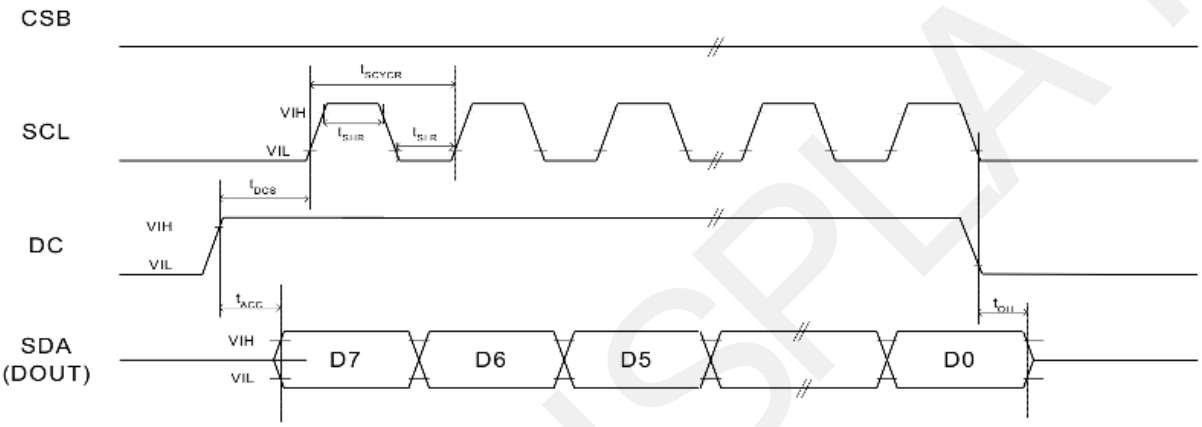
3-wire SPI characteristics (write mode)



3-wire SPI characteristics (read mode)



4-wire SPI characteristics (write mode)



4-wire SPI characteristics (read mode)

7. Command Table

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	00	0	0	0	0	0	0	0	0	PSR	Panel Setting Register A[7:0] = 2Fh [POR] B[7:0] = 09h [POR]
0	1		A_7	A_6	A_5	0	A_3	A_2	A_1	A_0		A[7:6] ~ RES[1:0] Display Resolution setting (source x gate) 00b: Follow TRES setting: 176 x 296 (Default), Map1 01b: 128 x 296, Map2 10b: 128 x 250, Map2 11b: 112 x 204, Map2 Map1: • Source output from S0 to S175, Map2: • Source output from S8 to S167, • S0~S7, S168~S175, VBD [outer] are HIZ. *Remark: Inactive Gate outputs will be VGL for DRF and AMV. Inactive Source outputs will follow VCOM LUT output for DRF A[5] ~ B_mode Blanking Mode for voltage switching, the duration setting follow CDI. 0: Mode A Blanking time only for ACVCOM. 1: Mode B (Default) Blanking time for ACVCOM or switch mode of source power. A[3] ~ UD Gate Scan Direction: 0: Scan down. First line to Last line: Gn-1 … G0 1: Scan up. (Default) First line to Last line: G0 … Gn-1 A[2] ~ SHL Source Shift Direction: 0: Shift left. First data to Last data: Sn-1 … S0 1: Shift right. (Default) First data to Last data: S0 … Sn-1 A[1] ~ SHD_N Booster Switch: 0 : Booster off, register data are kept, and Source/VBD/Vcom are kept 0V or floating. 1 : Booster on. (Default) A[0] ~ RST_N Soft Reset: 0: The controller is reset. Reset all registers to their default value. Driver all function will be disabled. 1: Normal operation (Default). BUSY_N will output low during operation.

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		B[7] ~ LUT_EN 0: During reset, auto load LUT from MTP if it is valid. When PON/DRF, analog setting will follow the content of MTP. (Default) 1: During reset, no action to load LUT from MTP. When PON/DRF, analog setting will follow the content of MCU B[6:5] ~ FOPT[1:0] FOPT function 00b: NO effect. Scan 1 frame after waveform finished (Default) 01b: Will scan 1 frame same as last output (of LUT) after waveform finished. 10b: Will scan 1 frame with Floating output after waveform finished. 11b: No Scan after waveform finished (Power off floating) B[4] ~ VCMZ VCOM Hi-Z option 0: NO effect. (default) 1: VCOM is always floating. B[3] ~ TS_AUTO Temperature Sensor auto option 0: NO effect. 1: Before loading MTP, Temperature Sensor will be activated automatically one time. (default) B[2] ~ TIEG VGL power off option 0: NO effect. (default) 1: After power off booster, VGL will be tied to GND. B[1] ~ NORG VCOM display end GND option 0: NO effect. (default) 1: After refreshing display, VCOM is tied to GND before power off B[0] ~ VC_LUTZ VCOM display end floating option 0: NO effect. 1: After refreshing display, the output of VCOM is set to floating automatically (default)

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	PWR	Power setting Register A[5:0] = 07h [POR] B[7:0] = F0h [POR] C[6:0] = 00h [POR] D[6:0] = 00h [POR] E[6:0] = 00h [POR] F[6:0] = 00h [POR]
0	1		0	0	A_5	A_4	A_3	A_2	A_1	A_0		A[5] ~ BD_EN Border output level selection: Border level / BD_EN=0 (default) / BD_EN=1 00b / VCOM / VCOM 01b / VSH / VSH+DCVCOM 10b / VSL / VSL+DCVCOM 11b / VSH2 / VSH2+DCVCOM A[4:3] ~ reserved A[2] ~ VSC_EN Source LV power selection: 0: External source power for VSH2 pin. 1: Internal DCDC function for generate source power. (default)
0	1		1	1	1	1	0	0	B_1	B_0		
0	1		0	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		0	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		0	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		0	F_6	F_5	F_4	F_3	F_2	F_1	F_0		

A[1] ~ VS_EN
Source LV power selection:
0: External source power for VSH1 and VSL pin.
1: Internal DCDC function for generate source power. (default)
A[0] ~ VG_EN
Gate power selection:
0: External gate power for VGH and VGL pin.
1: Internal DCDC function for generate gate power. (default)

B[1:0] ~ VGPN [1:0]
Internal VGH / VGL Voltage Level Selection:

VGPN [1:0]	Gate Voltage Level
00b	VGH=20V,VGL=-20V (Default) VSH=15V, VSL=-15V
01b	VGH=17V ,VGL=-17V VSH=15V, VSL=-15V
10b	VGH=15V,VGL=-15V VSH=13V, VSL=-13V
11b	Reserved.

C[6:0] ~ VSPL [6:0]
Internal Source Voltage Level Selection for VSH2@Mode0
D[6:0] ~ VSNL[6:0]
Internal Source Voltage Level Selection for VSL@Mode1
E[6:0] ~ VSPL2[6:0]
Internal Source Voltage Level Selection for VSH@Mode1
F[6:0] ~ VSNL2[6:0]
Internal Source Voltage Level Selection for VSH2@Mode1

Mode0: VSH=15V, VSL=-15V, VSH2=3~15V
Mode1: VSH=3~15V, VSL=-3~-15V, VSH2=3~15V

*Remark:
1. If VGH/VGL <+/-15V,
VSH/VSH2/VSL (max) = (VGH-2V / VGL+2V)
2. VSH ≥ VSH2

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description

VSPL[6:0]/VSPL2[6:0]/VSNL2[6:0]:

[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage
00h	3.0V	14h	5.0V	28h	7.0V	3Ch	9.0V	50h	11.0V	64h	13.0V	78h	15.0V
01h	3.1V	15h	5.1V	29h	7.1V	3Dh	9.1V	51h	11.1V	65h	13.1V		
02h	3.2V	16h	5.2V	2Ah	7.2V	3Eh	9.2V	52h	11.2V	66h	13.2V		
03h	3.3V	17h	5.3V	2Bh	7.3V	3Fh	9.3V	53h	11.3V	67h	13.3V		
04h	3.4V	18h	5.4V	2Ch	7.4V	40h	9.4V	54h	11.4V	68h	13.4V		
05h	3.5V	19h	5.5V	2Dh	7.5V	41h	9.5V	55h	11.5V	69h	13.5V		
06h	3.6V	1Ah	5.6V	2Eh	7.6V	42h	9.6V	56h	11.6V	6Ah	13.6V		
07h	3.7V	1Bh	5.7V	2Fh	7.7V	43h	9.7V	57h	11.7V	6Bh	13.7V		
08h	3.8V	1Ch	5.8V	30h	7.8V	44h	9.8V	58h	11.8V	6Ch	13.8V		
09h	3.9V	1Dh	5.9V	31h	7.9V	45h	9.9V	59h	11.9V	6Dh	13.9V		
0Ah	4.0V	1Eh	6.0V	32h	8.0V	46h	10.0V	5Ah	12.0V	6Eh	14.0V	Other	Reserved
0Bh	4.1V	1Fh	6.1V	33h	8.1V	47h	10.1V	5Bh	12.1V	6Fh	14.1V		
0Ch	4.2V	20h	6.2V	34h	8.2V	48h	10.2V	5Ch	12.2V	70h	14.2V		
0Dh	4.3V	21h	6.3V	35h	8.3V	49h	10.3V	5Dh	12.3V	71h	14.3V		
0Eh	4.4V	22h	6.4V	36h	8.4V	4Ah	10.4V	5Eh	12.4V	72h	14.4V		
0Fh	4.5V	23h	6.5V	37h	8.5V	4Bh	10.5V	5Fh	12.5V	73h	14.5V		
10h	4.6V	24h	6.6V	38h	8.6V	4Ch	10.6V	60h	12.6V	74h	14.6V		
11h	4.7V	25h	6.7V	39h	8.7V	4Dh	10.7V	61h	12.7V	75h	14.7V		
12h	4.8V	26h	6.8V	3Ah	8.8V	4Eh	10.8V	62h	12.8V	76h	14.8V		
13h	4.9V	27h	6.9V	3Bh	8.9V	4Fh	10.9V	63h	12.9V	77h	14.9V		

VSNL[6:0]:

[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage	[6:0]	Voltage
00h	-3.0V	14h	-5.0V	28h	-7.0V	3Ch	-9.0V	50h	-11.0V	64h	-13.0V	78h	-15.0V
01h	-3.1V	15h	-5.1V	29h	-7.1V	3Dh	-9.1V	51h	-11.1V	65h	-13.1V		
02h	-3.2V	16h	-5.2V	2Ah	-7.2V	3Eh	-9.2V	52h	-11.2V	66h	-13.2V		
03h	-3.3V	17h	-5.3V	2Bh	-7.3V	3Fh	-9.3V	53h	-11.3V	67h	-13.3V		
04h	-3.4V	18h	-5.4V	2Ch	-7.4V	40h	-9.4V	54h	-11.4V	68h	-13.4V		
05h	-3.5V	19h	-5.5V	2Dh	-7.5V	41h	-9.5V	55h	-11.5V	69h	-13.5V		
06h	-3.6V	1Ah	-5.6V	2Eh	-7.6V	42h	-9.6V	56h	-11.6V	6Ah	-13.6V		
07h	-3.7V	1Bh	-5.7V	2Fh	-7.7V	43h	-9.7V	57h	-11.7V	6Bh	-13.7V		
08h	-3.8V	1Ch	-5.8V	30h	-7.8V	44h	-9.8V	58h	-11.8V	6Ch	-13.8V		
09h	-3.9V	1Dh	-5.9V	31h	-7.9V	45h	-9.9V	59h	-11.9V	6Dh	-13.9V		
0Ah	-4.0V	1Eh	-6.0V	32h	-8.0V	46h	-10.0V	5Ah	-12.0V	6Eh	-14.0V	Other	Reserved
0Bh	-4.1V	1Fh	-6.1V	33h	-8.1V	47h	-10.1V	5Bh	-12.1V	6Fh	-14.1V		
0Ch	-4.2V	20h	-6.2V	34h	-8.2V	48h	-10.2V	5Ch	-12.2V	70h	-14.2V		
0Dh	-4.3V	21h	-6.3V	35h	-8.3V	49h	-10.3V	5Dh	-12.3V	71h	-14.3V		
0Eh	-4.4V	22h	-6.4V	36h	-8.4V	4Ah	-10.4V	5Eh	-12.4V	72h	-14.4V		
0Fh	-4.5V	23h	-6.5V	37h	-8.5V	4Bh	-10.5V	5Fh	-12.5V	73h	-14.5V		
10h	-4.6V	24h	-6.6V	38h	-8.6V	4Ch	-10.6V	60h	-12.6V	74h	-14.6V		
11h	-4.7V	25h	-6.7V	39h	-8.7V	4Dh	-10.7V	61h	-12.7V	75h	-14.7V		
12h	-4.8V	26h	-6.8V	3Ah	-8.8V	4Eh	-10.8V	62h	-12.8V	76h	-14.8V		
13h	-4.9V	27h	-6.9V	3Bh	-8.9V	4Fh	-10.9V	63h	-12.9V	77h	-14.9V		

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	02	0	0	0	0	0	0	1	0	POF	Power OFF Command Register
0	1		0	0	0	0	0	0	0	0		After power off command, driver will power off based on the Power OFF Sequence. BUSY_N will output low during operation. The Power OFF command will turn off DCDC, source driver, gate driver, VCOM driver, temperature sensor, but register and SRAM data will keep until VDD off. SD output will base on previous condition. *Remark: POF works at PON only
0	0	03	0	0	0	0	0	0	1	1	POFS	Power on/off Sequence Setting Register A[7:0] = 00h [POR]
0	1		0	0	A_5	A_4	0	0	A_1	A_0		A[5:4] ~ T_VDPG_OFF[1:0] Power off delay from VGH to VGL 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b: 80ms A[1:0] ~ T_VDS_OFF[1:0] Power off delay from VSHX/VSL to VGH 00b: 20ms (default) 01b: 40ms 10b: 60ms 11b : 80ms
0	0	04	0	0	0	0	0	1	0	0	PON	Power ON Command Register After the Power ON command, driver will power on based on the Power ON Sequence. BUSY_N will output low during operation. * Remark: PON Include booster on, VSH1/VSH2/VSL regulator on With default BTST, timing is >80ms

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	06	0	0	0	0	0	1	1	0	BTST	VGH Booster Soft Start Setting Register (for VGH) A[3:0] = 0Fh [POR] B[5:0] = 04h [POR] C[5:0] = 0Bh [POR] D[5:0] = 10h [POR] E[5:0] = 0Eh [POR] F[5:0] = 10h [POR] G[5:0] = 05h [POR]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		A[3:2] ~ T_VGHSSA [1:0] = 11 (Default) VGH booster soft start Phase A duration A[1:0] ~ T_VGHSSB [1:0] = 11 (Default) VGH booster soft start Phase B duration
0	1		0	0	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		0	0	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		0	0	E_5	E_4	E_3	E_2	E_1	E_0		
0	1		0	0	F_5	F_4	F_3	F_2	F_1	F_0		
0	1		0	0	G_5	G_4	G_3	G_2	G_1	G_0		
0	0	07	0	0	0	0	0	1	1	1	DSLP	Deep Sleep Register
0	1		1	0	1	0	0	1	0	1		This command makes the chip enter the deep-sleep mode. The deep sleep mode could return to stand-by mode by hardware reset assertion. The only one parameter is a check code, the command would be executed if check code is A5h.

Soft Start Phase Period (ms)
00b: 10
01b: 20
10b: 30
11b: 40

B[5:0] ~ VGHSSA_DRV [5:0] = 000100b (Default)
VGH Phase A Driving Strength
C[5:0] ~ VGHSSA_OFFT[[5:0] = 001011b (Default)
VGH Phase A Minimum OFF Time

D[5:0] ~ VGHSSB_DRV [5:0] = 010000b (Default)
VGH Phase B Driving Strength
E[5:0] ~ VGHSSB_OFFT[[5:0] = 001110b (Default)
VGH Phase B Minimum OFF Time

F[5:0] ~ VGHSSC_DRV [5:0] = 010000b (Default)
VGH Phase C Driving Strength
G[5:0] ~ VGHSSC_OFFT[[5:0] = 000101b (Default)
VGH Phase C Minimum OFF Time

Driving strength setting from strength1 to strength64 (strongest)

Minimum OFF Time (setting) from Period1 to Period64 (longest)

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	DTM	Data Start transmission Register
2 bit per pixel												This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.
0	1		KPixel1 [1:0]		KPixel2 [1:0]		KPixel3 [1:0]		KPixel4 [1:0]			
:			...									
0	1		KPixel (4M-3) [1:0]		KPixel (4M-2) [1:0]		KPixel (4M-1) [1:0]		KPixel (4M) [1:0]			

KPixel[1:0] Source Driver Output

	DDX=1 (Default)	DDX=0
00b	Gray 0	Gray 3
01b	Gray 1	Gray 2
10b	Gray 2	Gray 1
11b	Gray 3	Gray 0

After issue this command, the host must send at least 1-byte data to the device.

0	0	12	0	0	0	1	0	0	1	0	DRF	Display Refresh Command Register
0	1		0	0	0	0	0	0	0	0		After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. BUSY_N will output low during operation.
0	0	17	0	0	0	1	0	1	1	1	AUTO	Auto Sequence Register
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		This command makes the chip enter the auto sequence Single-chip application ONLY. Auto Sequence Option 0xA5: Start Auto Sequence (PON > DRF > POF) 0xA7: Start Auto Sequence (PON > DRF > POF > DSLP). Others: No effect BUSY_N will output low during operation.
0	0	30	0	0	1	1	0	0	0	0	PLL	Frame Rate Control register The command controls the clock frequency. A[3:0] = 2h [POR]
0	1		0	0	0	0	A_3	A_2	A_1	A_0		A[3] ~ Dyna Dynamic Frame Rate 0: Disable (Default) 1: Enable A[2:0] ~ FR[2:0] It supports the following frame rates. Frame Rate Selection, Frame rate for Gate/Source switching that exclude the blanking time defined in CDI.

FR[2:0]	Frame Rate Selection
000	12.5Hz
001	25Hz
010	50Hz (Default)
011	65Hz
100	75Hz
101	85Hz
110	100Hz
111	120Hz

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	40	0	1	0	0	0	0	0	0	TSC	Temperature Sensor Command Register
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		This command enables internal temperature sensor. BUSY_N will output low during operation. Then the temperature value can be read in 1degC step A[7:0] ~ TS[7:0]

TS[7:0]:

A[7:0]	Value(°C)	A[7:0]	Value(°C)	A[7:0]	Value(°C)	A[7:0]	Value(°C)	A[7:0]	Value(°C)
E7h	-25	F7h	-9	07h	7	17h	23	27h	39
E8h	-24	F8h	-8	08h	8	18h	24	28h	40
E9h	-23	F9h	-7	09h	9	19h	25	29h	41
EAh	-22	FAh	-6	0Ah	10	1Ah	26	2Ah	42
EBh	-21	FBh	-5	0Bh	11	1Bh	27	2Bh	43
ECh	-20	FCh	-4	0Ch	12	1Ch	28	2Ch	44
EDh	-19	FDh	-3	0Dh	13	1Dh	29	2Dh	45
EEh	-18	FEh	-2	0Eh	14	1Eh	30	2Eh	46
EFh	-17	FFh	-1	0Fh	15	1Fh	31	2Fh	47
F0h	-16	00h	0	10h	16	20h	32	30h	48
F1h	-15	01h	1	11h	17	21h	33	31h	49
F2h	-14	02h	2	12h	18	22h	34	32h	50
F3h	-13	03h	3	13h	19	23h	35	Other	Reserved
F4h	-12	04h	4	14h	20	24h	36		
F5h	-11	05h	5	15h	21	25h	37		
F6h	-10	06h	6	16h	22	26h	38		

0	0	41	0	1	0	0	0	0	0	1	TSE	Temperature Sensor Enable Register This command selects Temperature offset A[7:0] = 00h [POR]
0	1		0	0	0	0	A_3	A_2	A_1	0		A[3:0] ~ TO[3:1] , Temperature offset:

TO[3:1]	Calculation	TO[3:1]	Calculation
000b	+0	100b	-4
001b	+1	101b	-3
010b	+2	110b	-2
011b	+3	111b	-1

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	50	0	1	0	1	0	0	0	0	CDI	VCOM and DATA interval setting Register This command indicates the Border Output Selection and the interval between Vcom and data output A[7:0] = 97h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:5]~VBD [2:0] Border Output Selection:

	DDX=1	DDX=0
VBD[2:0]	LUT (Default)	LUT
000b	Gray 0	HIZ
001b	Gray 1	Gray 3
010b	Gray 2	Gray 2
011b	Gray 3	Gray 1
100b	HIZ(Default)	Gray 0

A[4]: DDX
Data Polarity for Pixel Data (See DTM command)
0: Invert
1: Non-invert (Default)

A[3:0] ~ CDI[3:0]
Gate and source blanking time (No gate source scanning)

CDI [3:0]	Interval (ms)	CDI [3:0]	Interval (ms)
0h	2	8h	40
1h	4	9h	60
2h	8	Ah	80
3h	12	Bh	100
4h	14	Ch	120
5h	16	Dh	140
6h	18	Eh	160
7h	20 (Default)	Fh	Reserved

User needs to review CDI setting to have stable VCOM in application

0	0	51	0	1	0	1	0	0	0	1	LPD	Lower Power Detection Register
1	1		0	0	0	0	0	0	0	A_0		BUSY_N will output low during operation. Then the LPD status can be read. A[0] ~ LPD status 0: Low power input VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL 1: Normal (default)

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	60	0	1	1	0	0	0	0	0	TCON	TCON setting Register This command defines non-overlap period of Gate and Source. A[7:0] = 04h [POR] B[7:0] = 02h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[5:0] ~ S2G[5:0] Source to Gate Non-overlap period B[5:0] ~ G2S[5:0] Gate to Source Non-overlap period
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

D[5:0]	S2G	G2S
00h	Reserved	3 unit
01h	Reserved	4 unit
02h	2 unit	5unit (Default)
03h	3 unit	6 unit
04h	4 unit (Default)	7 unit
05h	5 unit	8 unit
…	…	…
3Fh	63 unit	66 unit

Each time unit: ~0.5us

Remark:
Gate on time = line period – S2G – G2S
Min. Gate on time = 2unit
S2G + G2S ≤ line period – Min. Gate on time

0	0	61	0	1	1	0	0	0	0	1	TRES	Resolution setting Register A[7:0] = B0h [POR] B[8:0] = 128h [POR]
0	1		0	0	0	0	0	0	0	0		This command defines alternative resolution A[7:0] ~ HRES[7:0] Horizontal Display Resolution Remark: Horizontal resolution should be 4-multiple.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		B[8:0] ~ VRES[8:0] Vertical Display Resolution Remark: Vertical resolution should be 2-multiple.

e.g. HRES= B0h, VRES= 128h

UD,SHL	Source and gate sequence
00	S175,G295 to S0,G0
01	S0, G295 to S175,G0
10	S175,G0 to S0, G295
11	S0,G0 to S175, G295

Remark:
1) TRES is selected when PSR.RES=2'b00
2) VRES[8:0] >= 152

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	62	0	1	1	0	0	0	1	0	HTOTAL	HTOTAL setting Register. This command defines line time for different frame rate. A[7:0] = 0x44 [POR], B[7:0] = 0x38 [POR]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Which defined the line time for HTOTAL_A to HTOTAL_B respectively. Frame time = HTOTAL timing x TRES.VRES[8:0] Timing of POR is matched for VRES = 296.
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		Remark: 1) HTOTAL is effective when PSR.RES=2'b00 2) If user used TRES to define resolution, it needs to set the corresponding HTOTAL. Please refer to application note for details setting.

0	0	65	0	1	1	0	0	1	0	1	GSST	Gate/Source Start Setting Register. A[7:0] = 00h [POR] B[8:0] = 000h [POR]
0	1		0	0	0	0	0	0	0	0		A[7:0] ~ S_start[7:0] First valid source output channel setting
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	B_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

S_start [7:0]	First valid source output
00h	S0 (Default)
04h	S4
08h	S8
...	...
A8h	S168
ACh	S172
Other	Reserved

B[8:0] ~ G_start[8:0]
First valid gate output channel setting

GSST and TRES can define the display window from target source and gate start and end line.
Eg. GD: First G active = G16, G_start[8:0]=16.
Last G active = G279, VRES[8:0]=264.
SD: First S active = S8, S_start[7:0]=8.
Last S active = S167, HRES[7:0]=160.

Remark:
1) PSR.RES[1:0] = 00 (Map1)
2) G_start+VRES< 296, S_start+HRES< 176.

0	0	70	0	1	1	1	0	0	0	0	REV	Chip Revision Register The command is to read the ID A[7:0] = C3 [POR] B[7:0] = 01h [POR] C[7:0] = 01h [POR]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	80	1	0	0	0	0	0	0	0	AMV	Auto Measurement VCOM Register This command implements related VCOM sensing setting. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	0	A_0		A[7:6] ~ P[1:0] Number of sensing Points 00: 2 (Default) 01: 4 10: 8 11: 16 A[5:4] ~AMVT[1:0] Auto Measure Vcom Time: Sensing Time 00: 5 sec. (Default) 01: 10 sec. 10: 15 sec. 11: 20 sec. A[3] ~ AMVX VCOM measurement Gate settings 0: Gate scan normally during VCOM measurement (Default) 1: All Gates ON during VCOM measurement A[2] ~ AMVS Source output of AMV: 0: Set Source output to 0V during Auto Measure VCOM period. (Default) 1: Set Source output to VSH2 during Auto Measure VCOM period. A[0] ~ AMVE Auto Measure Vcom Enable (/Disable): 0: Disabled (Default) 1: Enabled BUSY_N will output low during operation. Note: AMV works at PON only

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	81	1	0	0	0	0	0	0	1	VV	Auto Measurement VCOM Register This command gets the Vcom value after AMV.
1	1		1	A_6	A_5	A_4	A_3	A_2	0	0		A[6:0] ~ VV[6:0]: Vcom read Value , valid range from -0.2V to -4.0V.

VV[6:0]:

A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage
04h	-0.2V	18h	-1.2V	2Ch	-2.2V	40h	-3.2V	Other	Reserved
06h	-0.3V	1Ah	-1.3V	2Eh	-2.3V	42h	-3.3V		
08h	-0.4V	1Ch	-1.4V	30h	-2.4V	44h	-3.4V		
0Ah	-0.5V	1Eh	-1.5V	32h	-2.5V	46h	-3.5V		
0Ch	-0.6V	20h	-1.6V	34h	-2.6V	48h	-3.6V		
0Eh	-0.7V	22h	-1.7V	36h	-2.7V	4Ah	-3.7V		
10h	-0.8V	24h	-1.8V	38h	-2.8V	4Ch	-3.8V		
12h	-0.9V	26h	-1.9V	3Ah	-2.9V	4Eh	-3.9V		
14h	-1.0V	28h	-2.0V	3Ch	-3.0V	50h	-4.0V		
16h	-1.1V	2Ah	-2.1V	3Eh	-3.1V	Other	Reserved		

0	0	82	1	0	0	0	0	0	1	0	VDCS	VCM_DC Setting Register This command sets VCOM_DC value. A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	0		A[7] ~ MTP _VCM Vcom follow VDCS after RESET. 0: Disable (Default), auto load from MTP if it is valid. 1: Enable, VCOM value from the VDCS[6:0] A[6:0] ~ VDCS[6:0]: VCOM_DC Setting, 0.1V step from -0.2V to -4V.

VDCS[6:0]:

A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage	A[6:0]	Voltage
04h	-0.2V	18h	-1.2V	2Ch	-2.2V	40h	-3.2V	Other	Reserved
06h	-0.3V	1Ah	-1.3V	2Eh	-2.3V	42h	-3.3V		
08h	-0.4V	1Ch	-1.4V	30h	-2.4V	44h	-3.4V		
0Ah	-0.5V	1Eh	-1.5V	32h	-2.5V	46h	-3.5V		
0Ch	-0.6V	20h	-1.6V	34h	-2.6V	48h	-3.6V		
0Eh	-0.7V	22h	-1.7V	36h	-2.7V	4Ah	-3.7V		
10h	-0.8V	24h	-1.8V	38h	-2.8V	4Ch	-3.8V		
12h	-0.9V	26h	-1.9V	3Ah	-2.9V	4Eh	-3.9V		
14h	-1.0V	28h	-2.0V	3Ch	-3.0V	50h	-4.0V		
16h	-1.1V	2Ah	-2.1V	3Eh	-3.1V	Other	Reserved		

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	83	1	0	0	0	0	0	1	1	PTLW	PARTIAL WINDOW This command sets partial window address. A[7:0] = 00h [POR] B[7:0] = AFh [POR] C[8:0] = 000h [POR] D[8:0] = 127h [POR] E[7:0] = 00h [POR]
0	1		0	0	0	0	0	0	0	0		A[7:0] ~ HRST [7:0] Horizontal start address B[7:0] ~ HRED [7:0] Horizontal end address C[8:0] ~ VRST [8:0] Vertical start address D[8:0] ~ VRED [8:0] Vertical end address
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	C_8		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		0	0	0	0	0	0	0	D_8		

0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		E[0] ~ PMODE 0: disable partial mode (Default) 1: enable partial mode Gate scan both inside and outside of the partial window Valid range Conventional HRST: 0(000h) to 172(ACh) /step 4 HRED: 3(003h) to 175(AFh) /step 4 VRST: 0(000h) to 295(127h) /step 1 VRED: 0(000h) to 295(127h) /step 1 Requirement: 1) HRST [8:0]<= HRED [8:0] 2) VRST [8:0]<= VRED [8:0]
0	1		0	0	0	0	0	0	0	E_0		
0	0	90	1	0	0	1	0	0	0	0	PGM	Program Mode This command is to set MTP program mode After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leave the program mode BUSY_N will output low until PGM mode is ready.
0	0	91	1	0	0	1	0	0	0	1	APG	Active Program This command is to execute MTP program After this command is issued, the chip would program the MTP. BUSY_N will output low during operation. Requirement: In PON mode with internal programming power.
0	0	92	1	0	0	1	0	0	1	0	RMTP	Read MTP Data
1	1		1st ~ dummy 2nd ~ N+1th Parameter									This command is to read the MTP content from SRAM. The 1st byte read is dummy byte. The 2nd byte read is the content of Address 0 in MTP The N+1th byte read is the content of Address n in MTP After issue this command, the host must read at least 1 byte data from the device.

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	93	1	0	0	1	0	0	1	1	RSRAM	Read SRAM Data This command is to read the content from SRAM. The 1st byte read is dummy byte. The 2nd byte read is the content of Address 0 in SRAM. The N+1th byte read is the content of Address n in SRAM. After issue this command, the host must read at least 1 byte data from the device.
1	1		1st ~ dummy 2nd ~ N+1th Parameter									
0	0	A2	1	0	1	0	0	0	1	0	PGM_CFG	MTP Program Config This command is to set the configuration of MTP
0	1		0	0	1	1	0	A_2	A_1	A_0		A[2:0] ~ PGM_UMODE[2:0] 000b: Reserved 001b: Compressed LUT (Default) 010b: Init Code Others: Reserved B[7:0] ~ PGM_SADDR[15:8], C[7:0] ~ PGM_SADDR[7:0] Program Start Address: Compressed LUT: 0000h Init Code: 0000h D[7:0] ~ PGM_DSIZE [15:8] E[7:0] ~ PGM_DSIZE [7:0] Program data size in bytes
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	1		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	1		E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		

0	0	A3	1	0	1	0	0	0	1	1	PGM_STAT	MTP Program Status This command is to read MTP Program status A[7:0] = 00h [POR]
1	1		0	0	0	0	0	0	A_1	A_0		A[1] ~ PGM_VER_ERR Data verification of APG 0: OK 1: NOK A[0] ~ PGM_EXE_ERR MTP program execution status 0: Normal 1: Invalid APG setting
0	0	A4	1	0	1	0	0	1	0	0	MTP_STAT	MTP Status Register This command is to read MTP status A[7:0] = 00h [POR] B[7:0] = 00h [POR]
1	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7] ~ LUT_TYPE[7] User MTP Type 0: Blank 1: Compressed
0	0	E0	1	1	1	0	0	0	0	0	CCSET	CCSET for temperature input selection A[7:0] = 00h [POR]
0	1		0	0	0	0	0	0	A_1	0		A[1] = TSFIX Temperature Input selection 0: Use Internal Temperature sensor (Default) 1: Use TSSET[7:0] value

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	E3	1	1	1	0	0	0	1	1	PWS	Power Saving Register This command is sets for saving power VCOM/Source power saving during display refresh period. A[7:0] = 65h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		If the output voltage of VCOM/Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters. A[7:4] = VCOM_W [3:0]

VCOM_W [3:0]	VCOM_power saving width. (time unit)	VCOM_W [3:0]	VCOM_power saving width. (time unit)
0	Reserved	8	8
1	1	9	9
2	2	10	10
3	3	11	11
4	4	12	12
5	5	13	13
6	6[Default]	14	14
7	7	15	15

A[3:0] = SD_W [3:0]

SD_W [3:0]	Source power saving width[us]	SD_W [3:0]	Source power saving width [us]
0	Reserved	8	4
1	0.5	9	4.5
2	1	10	5
3	1.5	11	5.5
4	2	12	6
5	2.5[Default]	13	6.5
6	3	14	7
7	3.5	15	7.5

*Remark:
VCOM_W setting < CDI setting
SD_W setting < S2G setting

0	0	E4	1	1	1	0	0	1	0	0	LVSEL	LVD Voltage Select Register This command is sets for low power detect level power A[1:0] = 3h [POR]
0	1		0	0	0	0	0	0	A_1	A_0		A[1:0] ~ LVD_SEL[1:0] Low power detection threshold 00: 2.2V 01: 2.3V 10: 2.4V 11 : 2.5V (Default)

R/W#	DC	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	E6	1	1	1	0	0	1	1	0	TSSET	Manual input temperature value This command is to force the TS value A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:0] ~ TS_SET[7:0] When TSFIX=1, Temperature value will be set by TS_SET[7:0]. Format of the temperature value is 8-bit binary value and it is 1°C per step.

TS_SET[7:0]:

A[7:0]	Value(°C)	A[7:0]	Value(°C)	A[7:0]	Value(°C)	A[7:0]	Value(°C)	A[7:0]	Value(°C)
E7h	-25	F7h	-9	07h	7	17h	23	27h	39
E8h	-24	F8h	-8	08h	8	18h	24	28h	40
E9h	-23	F9h	-7	09h	9	19h	25	29h	41
EAh	-22	FAh	-6	0Ah	10	1Ah	26	2Ah	42
EBh	-21	FBh	-5	0Bh	11	1Bh	27	2Bh	43
ECh	-20	FCh	-4	0Ch	12	1Ch	28	2Ch	44
EDh	-19	FDh	-3	0Dh	13	1Dh	29	2Dh	45
EEh	-18	FEh	-2	0Eh	14	1Eh	30	2Eh	46
EFh	-17	FFh	-1	0Fh	15	1Fh	31	2Fh	47
F0h	-16	00h	0	10h	16	20h	32	30h	48
F1h	-15	01h	1	11h	17	21h	33	31h	49
F2h	-14	02h	2	12h	18	22h	34	32h	50
F3h	-13	03h	3	13h	19	23h	35	Other	Reserved
F4h	-12	04h	4	14h	20	24h	36		
F5h	-11	05h	5	15h	21	25h	37		
F6h	-10	06h	6	16h	22	26h	38		

0	0	E7	1	1	1	0	0	1	1	1	PST	VGH Booster Soft Start Setting Register (for VGH) during switch mode A[5:0] = 10h [POR] B[5:0] = 05h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[5:0] ~ VGHSM_DRV [5:0] = 010000b (Default) VGH switch mode Driving Strength B[5:0] ~ VGHSM_OFFT[[5:0] = 000101b (Default) VGH switch mode Minimum OFF Time Remark: PSR.B_mode=1
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		

8. Optical Specifications

Measurements are made with the illumination at a 45-degree angle and the detection perpendicular to the surface, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
T update	Image update time	at 25 °C		26	-	sec	
Life		Topr		1000000times or 5years			

Notes: Luminance meter: Eye-One Pro Spectrophotometer.

8-1.8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

9. Handling, Safety and Environment Requirements

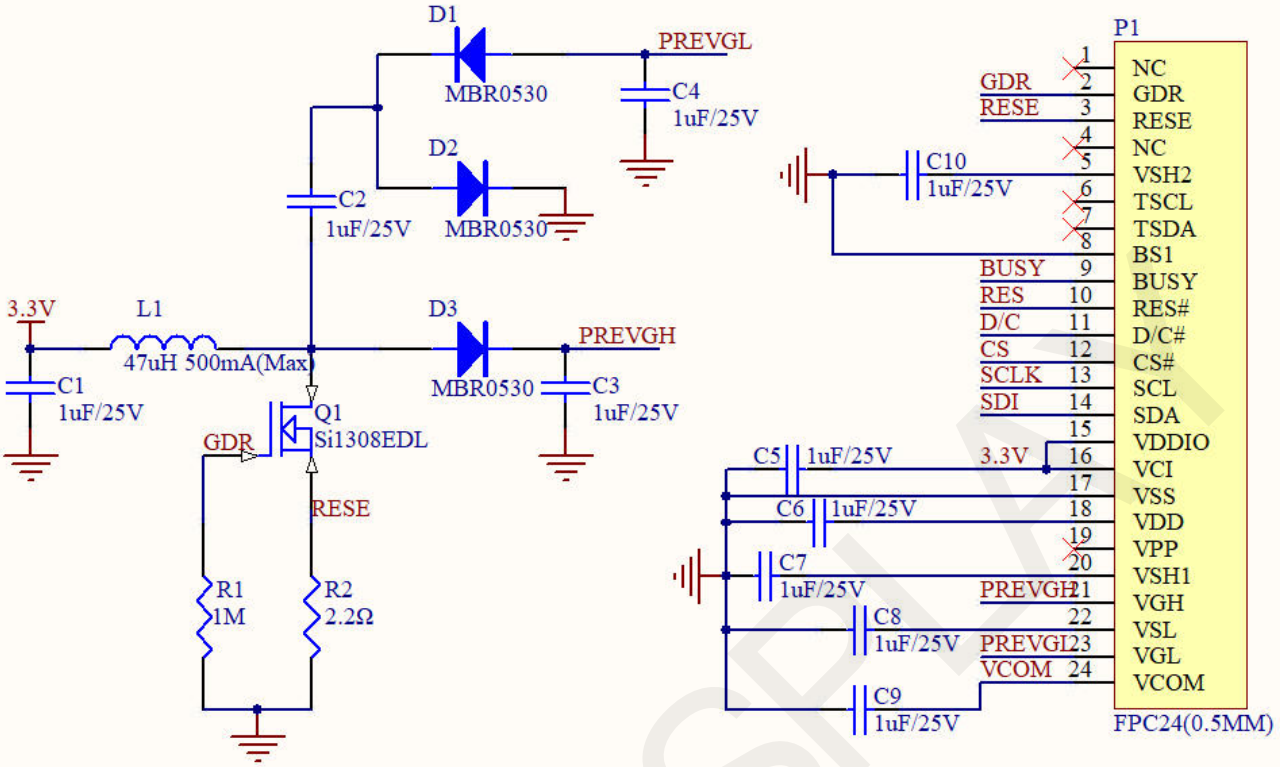
Warning
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.
Caution
The display module should not be exposed to harmful gases, such as aalkaligases,whichcorrodeelectronic components. Disassembling the display module. Disassembling the display module can cause permanent damage and invalidates the warranty agreements. Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.
Data sheet status
Product specification: This data sheet contains final product specifications.
Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and does not form part of the specification.

10. Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60° C，RH=35%，240h Test in white pattern
3	High-Temperature Operation	T=40° C，RH=35%，240h
4	Low-Temperature Operation	T=0° C，240h
5	High-Temperature, High-Humidity Operation	T=40° C，RH=80%，240h
6	High Temperature, High Humidity Storage	T=50° C，RH=90%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25℃ 30min]→[+60℃ 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

11. Typical Application Circuit



Part Name	Requirements for spare part
C1—C10	0603/0805; X5R/X7R;Voltage Rating:≥25V
R1、R2	0603/0805;1% variation,≥0.05W
D1—D3	MBR0530: 1)Reverse DC Voltage≥30V 2)Io≥500mA 3)Forward voltage ≤430mV
Q1	Si1308EDL:1)Drain-Source breakdown voltage≥30V 2)Vgs(th)≤1.5V 3)Rds(on)≤400mΩ
L1	refer to NR3015: Io=500mA(max)
P1	24pins,0.5mm pitch

1. The recommended component values and reference parts listed in the Table are subject to change depending on the panel loading conditions.

2. It is required that the customer review whether the selected component values and parts are suitable for their specific application.

12. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) Good Display 's E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.
DESPI Development Kit consists of the development board and the pinboard.

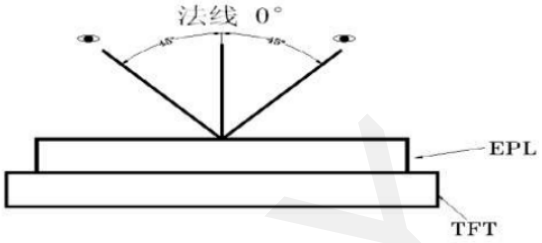
More details about the Development Kit, please click to the following link:

https://www.good-display.com/product/53/

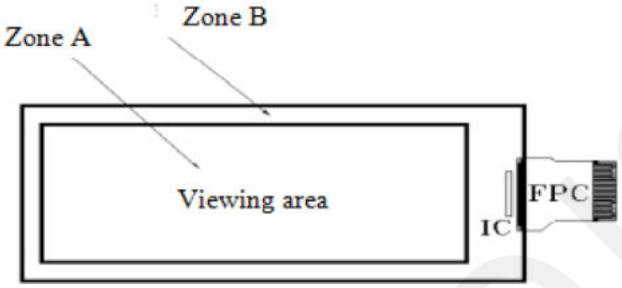
13. Inspection method and condition

13.1 Inspection condition

Item	Condition
Illuminance	800~1500 lux
Temperature	22℃±3℃
Humidity	55±10 %RH
Distance	≥30cm
Angle	Vertical fore and aft 45
Inspection method	By eyes

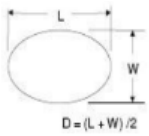


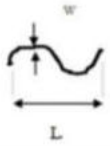
13.2 Display area

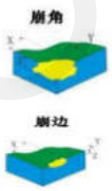
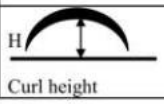


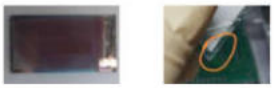
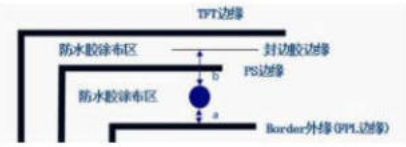
13. 3 General inspection standards for products

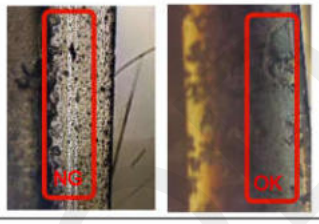
13.3.1 Appearance inspection standard

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Spot defects	Spot defects such as dot, foreign matter, air bubble, and dent etc.	Diameter D=(L+W)/2 (L-length、W-width) Measuring method shown in the figure below 	The distance between the two spots should not be less than 10mm	7.5"-13.3"Module（Not include 7.5"）： D>1mm N=0 0.5<D≤0.8 N≤4 D≤0.5 Ignore 0.8<D≤1 N≤2 4.2"-7.5"Module（Not include 4.2"）： D>0.5 N=0 0.4<D≤0.5 N≤2 D≤0.25 Ignore 0.25<D≤0.4 N≤4 Module below 4.2"： D>0.5 N=0 0.4<D≤0.5 N≤1 D≤0.25 Ignore 0.25<D≤0.4 N≤4 0.1mm<D≤0.25 N≤3/cm²	Foreign matter D≤1mm Pass	Check by eyes Film gauge	MIN

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Line defects	Line defects such as scratch, hair etc.	L-Length，W-Width，(W/L)<1/4 Judged by line， (W/L)≥1/4 Judged by dot 	The distance between the two lines should not be less than 5mm	7.5"-13.3"Module（Not include 7.5"）： L>10mm,N=0 W>0.8mm，N=0 5mm≤L≤10mm，0.5mm≤W≤0.8mm N≤2 L≤5mm，W≤0.5mm Ignore 4.2"-7.5"Module（Not include 4.2"）： L>8mm,N=0 W>0.2mm，N=0 2mm≤L≤8mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore Module below 4.2"： L>5mm,N=0 W>0.2mm，N=0 2mm≤L≤5mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore	Ignore	Check by eyes Film gauge	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Panel chipping and crack defects	TFT panel chipping	X the length, Y the width, Z the chipping height, T the thickness of the panel 	Chipping at the edge： Module over 7.5"（Include 7.5"）： X≤ 6mm,Y≤1mm Z≤T N=3 Allowed Module below 7.5"(Not include 7.5")： X≤ 3mm,Y≤1mm Z≤T N=3 Allowed Chipping on the corner： IC sideX≤2mm Y≤2mm, Non-IC sideX≤1mm Y≤1mm . Allowed Note： Chipping should not damage the edge wiring. If it does not affect the display, allowed	Check by eyes、 Film gauge	MIN
	Crack		Crack at any zone of glass , Not allowed	Check by eyes、Film gauge	MIN
	Burr edge		No exceed the positive and negative deviation of the outline dimensions X+Y≤0.2mm Allowed	Calliper	MIN
	Curl of panel		Curl height H≤Total panel length 1% Allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ / MIN
PS defect	Water proof film		1 .Waterproof film damage, wrinkled, open edge, not allowed 2. Exceeding the edge of module(according to the lamination drawing) Not allowed 3. Edge warped exceeds height of technical file, not allowed	Check by eyes	MIN
RTV defect	Adhesive effect		Adhesive height exceeds the display surface, not allowed	Check by eyes	MIN
			1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2 .No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3. No adhesive at edge and corner1*1mm, no exposure of wiring, allowed		
			Protection adhesive, coverage width within W≤1.5mm, no break of adhesive, allowed		
	Adhesive re-fill		Dispensing is uniform, without obvious concave and breaking, bubbling and swell, not higher than the upper surface of the PS, and the diameter of the adhesive re-filling is not more than 8mm, allowed	Check by eyes	MIN
EC defect	Adhesive bubble		1、 Effective edge sealing area of hot melt products ≥1/2 edge sealing area; 2、Bubble a+b≥1/2 effective width, N≤3, spacing≥5mm , allowed No exposure of wiring, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
EC defect	Adhesive effect		1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2.No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3.No adhesive at edge and corner 1*1mm, no exposure of wiring, allowed 4. Adhesive height exceeds the display surface, not allowed	Visual, caliper	MIN
Silver dot adhesive defect	Silver dot adhesive		1、Single silver dot dispensing amount ≥1mm, allowed 2、One of the double silver dot dispensing amount is ≥1mm and the other has adhesive (no reference to 1mm) Allowed	Visual	MIN
			Silver dot dispensing residue on the panel ≤0.2mm, allowed	Film gauge	MIN
FPC defect	FPC wiring		FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
	FPC golden finger		The height of burr edge of TCP punching surface ≅ 0.4mm, not allowed	Caliper	MIN
	FPC damage/crease		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Protective film defect	Protective film	Scratch and crease on the surface but no affect to protection function, allowed		Check by eyes	MIN
		Adhesive at edge L≤5mm，W≤0.5mm，N=2, no entering into viewing area		Check by eyes	MIN
Stain defect	Stain	If stain can be normally wiped clean by ≥ 99% alcohol, allowed		Visual	MIN
Pull tab defect	Pull tab	The position and direction meet the document requirements, and ensure that the protective film can be pulled off.		Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape	Tilt≤10°, flat without warping, completely covering the IC.		Check by eyes/ Film gauge	MIN
Stiffener	Stiffener	Flat without warping, Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than 0.5mm from FPC edge		Check by eyes	MIN
Label	Label/ Spraying code	The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.		Check by eyes	MIN

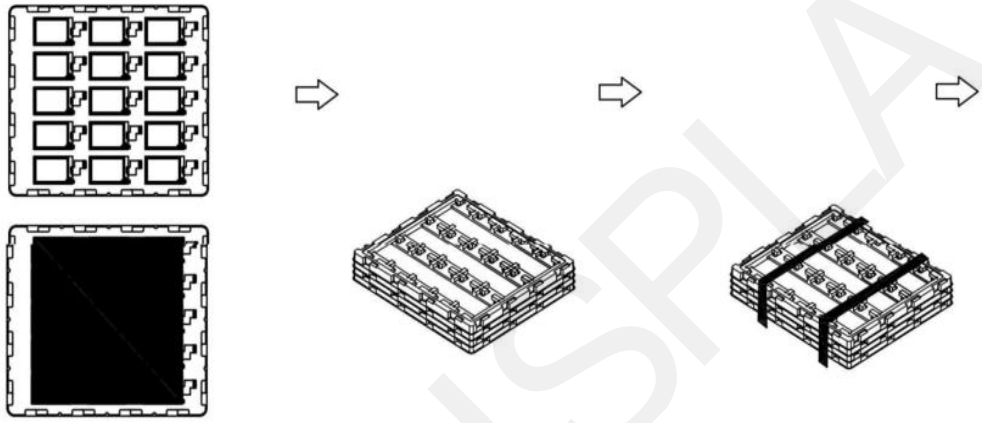
14. Packing

PACKLING ORDER:

1) Putting 28 pcs Modules on each PET tray.And cover a dedicated EPE film.

2) Putting 9 pcs PET trays together with 1 empty tray on the top of PET tray.

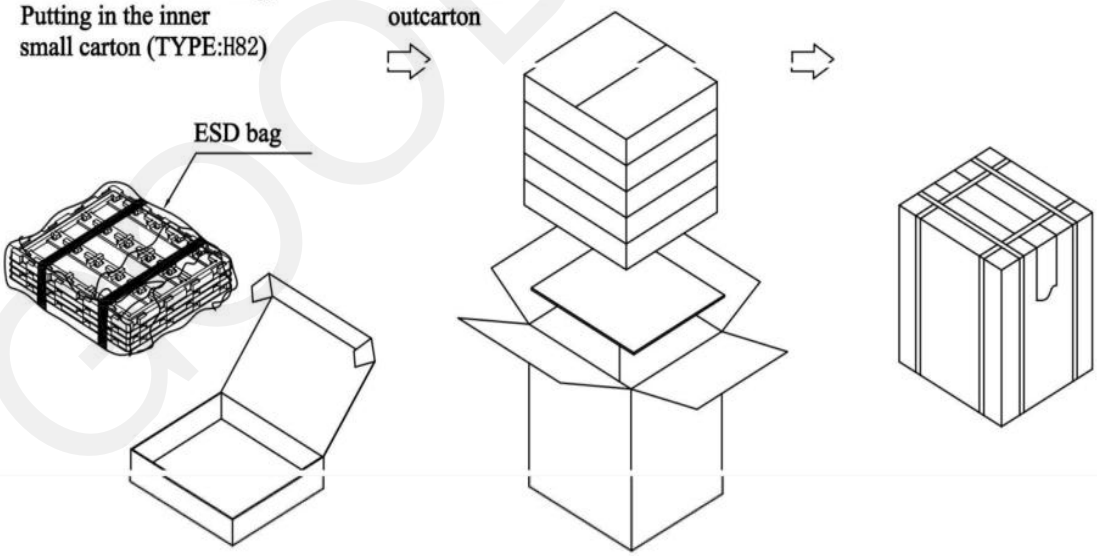
3) the tray together with rubber band



4) Insert in the ESD bag, add desiccant in the ESD bag, Putting in the inner small carton (TYPE:H82)

5) Putting 5 small cartons into one outcarton

6) Packing finished



Note: 28pcs in a tray, 9 trays in a inner carton, 5 inner cartons in a out carton, so 28x(10-1)x5=1260pcs/Outcarton

Dimension (Small carton): 385*325*87mm Dimension (Out carton): 394*344*470mm

15. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

(6) For more precautions, please click on the link:

https://www.good-display.com/news/80.html