Specification

資料中心參考文件用章
For Reference Only
2024.12.20
聯合聚晶股份有限公司
Integrated Solution Technology, Inc

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
Research & Development	Jeff 2024/12/20	Henry Tsai 2024/12/20	Bonnie Lee 2024/12/20

Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
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文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
001	-	New release	E122400021	Jeff	2024/12/20

續頁 CONTINUATION --- ☐ 是 YES; ☒ 否 NO

THIS CHIP HAS BEEN VERIFIED BY E INK ™ AND GOT E INK'S FULL 2BIT-E5 AUTHORIZATION.

This driver is an Active Matrix EPD all-in-one driver with timing controller for ESL. The sources have 2-bit outputs per pixel to support white/black/color. The timing controller provides control signals for the source driver and external gate drivers.

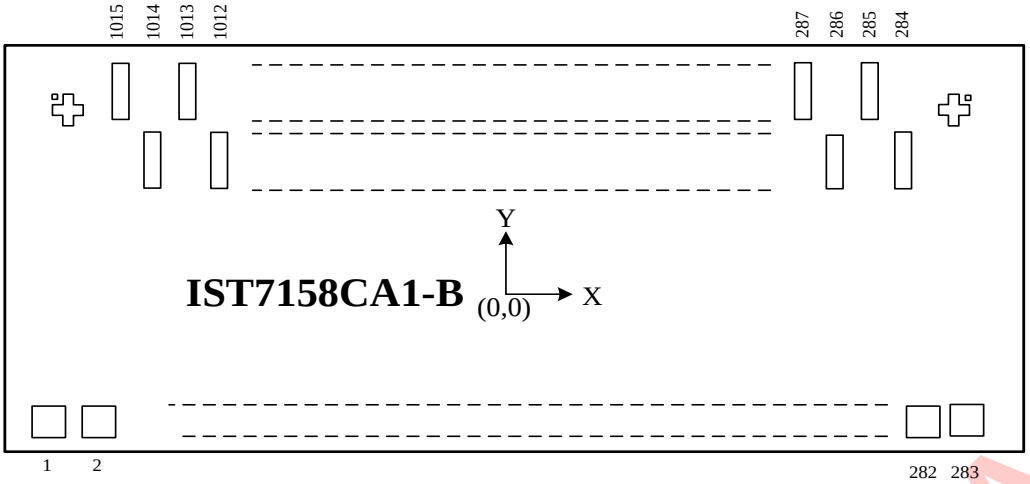
The DC-DC controller allows generate all necessary source and gate output voltage for VDH/VDL/VDHR (+/-3V~+/-15V), and VGH/VGL (+/-20v, +/-17v, +/-15v, +/-10v). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

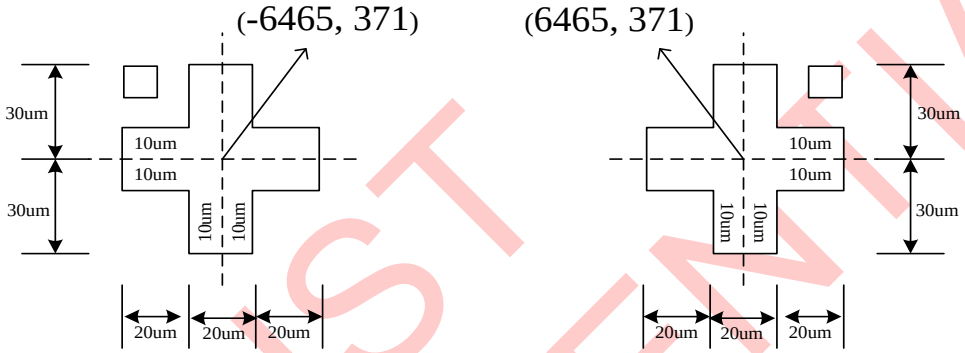
FEATURES

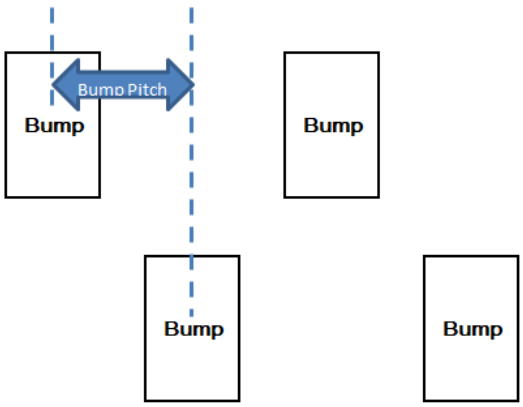
- System-on-chip (SOC) for ESL
- Timing controller support several all resolution
- Resolution: Support 400S x 300G
  - 400 Outputs source driver with 2-bit white/black/color per pixel
    - Output dynamic range (Voltage step: 100mV)
      - Mode 0 : 0V & VDH (+15V) & VDL (-15V) & VDHR (+3V~+15V)
      - Mode 1 : 0V & VDH (+3V~+15V) & VDL (-3V~-15V) & VDHR1 (+3V~+15V)
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame)
    - Left and Right shift capability
  - 300 Output Gate drive
    - Output dynamic range: VGH and VGL: +/-20v, +/-17v, +/-15v, +/-10v
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
    - VCOMH=VDH+VCOMDC, VCOML=VDL+VCOMDC
  - Support sensing function
  - Support LUT
- Border electrode level
    - 0V+VCOMDC & VDH+VCOMDC & VDL+VCOMDC & VDHR+VCOMDC & HiZ
- Builtin frame memory maximum: (400 x300x2bits)x1 SRAM
- Builtin temperature sensor
  - On-Chip:On-Chip:-25~50°C (±2.0 °C)/8-bit status

- Support LPD, Low Power detection (VDD<2.5V)
- Support frame rate: 120Hz (max)
- 3-wire/4-wire (SPI) serial interface for system configuration: Clock rate up to 20MHz
- Digital supply voltage: 2.3~3.6V
- On-chip OTP for LUT and parameters (6K bytes)
- Support source cascade
- COG Package

PAD CONFIGURATION







Chip Size	13120 x 929um^2	
Bump Pitch	14um(min)	
Bump Size(X*Y)	28x 70 um^2	Pad No = 1 ~ 283
	17x75 um^2	Pad No = 284 ~ 446
	16x75 um^2	Pad No = 447 ~ 852
	17x75 um^2	Pad No = 853 ~ 1015
Bump Height	9um (Typ)	
Chip Thickness	300um (Typ)	

PAD CENTER COORDINATES

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
1	NC	-6486	-390	51	VGH	-4186	-390	101	VSS1	-1886	-390
2	NC	-6440	-390	52	VGH	-4140	-390	102	VSS1	-1840	-390
3	VCOM	-6394	-390	53	VGH	-4094	-390	103	VSS1	-1794	-390
4	VCOM	-6348	-390	54	VSS1	-4048	-390	104	VSS1	-1748	-390
5	VCOM	-6302	-390	55	VDH	-4002	-390	105	VSS1	-1702	-390
6	VCOM	-6256	-390	56	VDH	-3956	-390	106	VSS1	-1656	-390
7	VCOM	-6210	-390	57	VDH	-3910	-390	107	VDD3	-1610	-390
8	VCOM	-6164	-390	58	VDH	-3864	-390	108	VDD3	-1564	-390
9	VCOM	-6118	-390	59	VDH	-3818	-390	109	VDD3	-1518	-390
10	VCOM	-6072	-390	60	VDH	-3772	-390	110	VDD1	-1472	-390
11	VSS4	-6026	-390	61	VDH	-3726	-390	111	VDD1	-1426	-390
12	VGL	-5980	-390	62	VDH	-3680	-390	112	VDD1	-1380	-390
13	VGL	-5934	-390	63	VDH	-3634	-390	113	VDD1	-1334	-390
14	VGL	-5888	-390	64	VDH	-3588	-390	114	VDD5	-1288	-390
15	VGL	-5842	-390	65	VSS1	-3542	-390	115	VDD5	-1242	-390
16	VGL	-5796	-390	66	VPP	-3496	-390	116	VDD5	-1196	-390
17	VGL	-5750	-390	67	VPP	-3450	-390	117	VDD2	-1150	-390
18	VGL	-5704	-390	68	VPP	-3404	-390	118	VDD2	-1104	-390
19	VGL	-5658	-390	69	VPP	-3358	-390	119	VDD2	-1058	-390
20	VGL	-5612	-390	70	VPP	-3312	-390	120	VDD2	-1012	-390
21	VGL	-5566	-390	71	VPP	-3266	-390	121	VDD2	-966	-390
22	VGL	-5520	-390	72	VPP	-3220	-390	122	VDD2	-920	-390
23	VGL	-5474	-390	73	VDDLO	-3174	-390	123	VDD2	-874	-390
24	VGL	-5428	-390	74	VDDLO	-3128	-390	124	NC	-828	-390
25	VGL	-5382	-390	75	VDDLO	-3082	-390	125	NC	-782	-390
26	VGL	-5336	-390	76	VDDLO	-3036	-390	126	NC	-736	-390
27	VGL	-5290	-390	77	VDDLO	-2990	-390	127	NC	-690	-390
28	VSS1	-5244	-390	78	VDDLI	-2944	-390	128	NC	-644	-390
29	VDL	-5198	-390	79	VDDLI	-2898	-390	129	NC	-598	-390
30	VDL	-5152	-390	80	VDDLI	-2852	-390	130	NC	-552	-390
31	VDL	-5106	-390	81	VDDLI	-2806	-390	131	NC	-506	-390
32	VDL	-5060	-390	82	VDDLI	-2760	-390	132	NC	-460	-390
33	VDL	-5014	-390	83	VSS3	-2714	-390	133	NC	-414	-390
34	VDL	-4968	-390	84	VSS3	-2668	-390	134	NC	-368	-390
35	VDL	-4922	-390	85	VSS2	-2622	-390	135	NC	-322	-390
36	VDL	-4876	-390	86	VSS2	-2576	-390	136	NC	-276	-390
37	VDL	-4830	-390	87	VSS2	-2530	-390	137	NC	-230	-390
38	VDL	-4784	-390	88	VSS2	-2484	-390	138	NC	-184	-390
39	VSS1	-4738	-390	89	VSS2	-2438	-390	139	NC	-138	-390
40	VGH	-4692	-390	90	VSS5	-2392	-390	140	NC	-92	-390
41	VGH	-4646	-390	91	VSS5	-2346	-390	141	NC	-46	-390
42	VGH	-4600	-390	92	VSS5	-2300	-390	142	NC	0	-390
43	VGH	-4554	-390	93	VSS5	-2254	-390	143	NC	46	-390
44	VGH	-4508	-390	94	VSS5	-2208	-390	144	NC	92	-390
45	VGH	-4462	-390	95	VSS4	-2162	-390	145	NC	138	-390
46	VGH	-4416	-390	96	VSS4	-2116	-390	146	NC	184	-390
47	VGH	-4370	-390	97	VSS4	-2070	-390	147	NC	230	-390
48	VGH	-4324	-390	98	VSS4	-2024	-390	148	NC	276	-390
49	VGH	-4278	-390	99	VSS4	-1978	-390	149	NC	322	-390
50	VGH	-4232	-390	100	VSS4	-1932	-390	150	NC	368	-390

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
151	NC	414	-390	201	NC	2714	-390	251	VDHR	5014	-390
152	NC	460	-390	202	NC	2760	-390	252	NC	5060	-390
153	NC	506	-390	203	VDDIO	2806	-390	253	NC	5106	-390
154	NC	552	-390	204	NC	2852	-390	254	NC	5152	-390
155	NC	598	-390	205	VSS1	2898	-390	255	NC	5198	-390
156	NC	644	-390	206	NC	2944	-390	256	NC	5244	-390
157	NC	690	-390	207	VDDIO	2990	-390	257	NC	5290	-390
158	NC	736	-390	208	BS	3036	-390	258	VSS1	5336	-390
159	NC	782	-390	209	VSS1	3082	-390	259	FB	5382	-390
160	NC	828	-390	210	NC	3128	-390	260	FB	5428	-390
161	NC	874	-390	211	VDDIO	3174	-390	261	VSS1	5474	-390
162	VSS1	920	-390	212	CPBI	3220	-390	262	RESE	5520	-390
163	NC	966	-390	213	VSS1	3266	-390	263	RESE	5566	-390
164	NC	1012	-390	214	MS	3312	-390	264	VSS1	5612	-390
165	NC	1058	-390	215	VDDIO	3358	-390	265	GDR	5658	-390
166	VDDIO	1104	-390	216	VSS1	3404	-390	266	GDR	5704	-390
167	VDDIO	1150	-390	217	TSDA	3450	-390	267	GDR	5750	-390
168	VDDIO	1196	-390	218	TSDA	3496	-390	268	GDR	5796	-390
169	VDDIO	1242	-390	219	TSCL	3542	-390	269	GDR	5842	-390
170	NC	1288	-390	220	TSCL	3588	-390	270	GDR	5888	-390
171	TESTIN1	1334	-390	221	VSS1	3634	-390	271	GDR	5934	-390
172	TESTIN2	1380	-390	222	CPBO	3680	-390	272	GDR	5980	-390
173	NC	1426	-390	223	NC	3726	-390	273	VSS4	6026	-390
174	TESTO1	1472	-390	224	VSS1	3772	-390	274	VCOM	6072	-390
175	TESTO2	1518	-390	225	NC	3818	-390	275	VCOM	6118	-390
176	NC	1564	-390	226	NC	3864	-390	276	VCOM	6164	-390
177	SDA	1610	-390	227	VSS1	3910	-390	277	VCOM	6210	-390
178	SCL	1656	-390	228	NC	3956	-390	278	VCOM	6256	-390
179	VSS1	1702	-390	229	NC	4002	-390	279	VCOM	6302	-390
180	CSB	1748	-390	230	VSS1	4048	-390	280	VCOM	6348	-390
181	VDDIO	1794	-390	231	NC	4094	-390	281	VCOM	6394	-390
182	NC	1840	-390	232	NC	4140	-390	282	NC	6440	-390
183	NC	1886	-390	233	VSS1	4186	-390	283	NC	6486	-390
184	VSS1	1932	-390	234	NC	4232	-390	284	NC	6345	294.5
185	A0	1978	-390	235	NC	4278	-390	285	NC	6324	394.5
186	VDDIO	2024	-390	236	NC	4324	-390	286	NC	6303	294.5
187	NC	2070	-390	237	NC	4370	-390	287	NC	6282	394.5
188	NC	2116	-390	238	NC	4416	-390	288	NC	6261	294.5
189	NC	2162	-390	239	NC	4462	-390	289	NC	6240	394.5
190	NC	2208	-390	240	NC	4508	-390	290	G<0>	6219	294.5
191	RESB	2254	-390	241	NC	4554	-390	291	G<2>	6198	394.5
192	BUSY_N	2300	-390	242	NC	4600	-390	292	G<4>	6177	294.5
193	VSS1	2346	-390	243	NC	4646	-390	293	G<6>	6156	394.5
194	NC	2392	-390	244	VDHR	4692	-390	294	G<8>	6135	294.5
195	NC	2438	-390	245	VDHR	4738	-390	295	G<10>	6114	394.5
196	NC	2484	-390	246	VDHR	4784	-390	296	G<12>	6093	294.5
197	NC	2530	-390	247	VDHR	4830	-390	297	G<14>	6072	394.5
198	NC	2576	-390	248	VDHR	4876	-390	298	G<16>	6051	294.5
199	CL	2622	-390	249	VDHR	4922	-390	299	G<18>	6030	394.5
200	NC	2668	-390	250	VDHR	4968	-390	300	G<20>	6009	294.5

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
301	G<22>	5988	394.5	351	G<122>	4938	394.5	401	G<222>	3888	394.5
302	G<24>	5967	294.5	352	G<124>	4917	294.5	402	G<224>	3867	294.5
303	G<26>	5946	394.5	353	G<126>	4896	394.5	403	G<226>	3846	394.5
304	G<28>	5925	294.5	354	G<128>	4875	294.5	404	G<228>	3825	294.5
305	G<30>	5904	394.5	355	G<130>	4854	394.5	405	G<230>	3804	394.5
306	G<32>	5883	294.5	356	G<132>	4833	294.5	406	G<232>	3783	294.5
307	G<34>	5862	394.5	357	G<134>	4812	394.5	407	G<234>	3762	394.5
308	G<36>	5841	294.5	358	G<136>	4791	294.5	408	G<236>	3741	294.5
309	G<38>	5820	394.5	359	G<138>	4770	394.5	409	G<238>	3720	394.5
310	G<40>	5799	294.5	360	G<140>	4749	294.5	410	G<240>	3699	294.5
311	G<42>	5778	394.5	361	G<142>	4728	394.5	411	G<242>	3678	394.5
312	G<44>	5757	294.5	362	G<144>	4707	294.5	412	G<244>	3657	294.5
313	G<46>	5736	394.5	363	G<146>	4686	394.5	413	G<246>	3636	394.5
314	G<48>	5715	294.5	364	G<148>	4665	294.5	414	G<248>	3615	294.5
315	G<50>	5694	394.5	365	G<150>	4644	394.5	415	G<250>	3594	394.5
316	G<52>	5673	294.5	366	G<152>	4623	294.5	416	G<252>	3573	294.5
317	G<54>	5652	394.5	367	G<154>	4602	394.5	417	G<254>	3552	394.5
318	G<56>	5631	294.5	368	G<156>	4581	294.5	418	G<256>	3531	294.5
319	G<58>	5610	394.5	369	G<158>	4560	394.5	419	G<258>	3510	394.5
320	G<60>	5589	294.5	370	G<160>	4539	294.5	420	G<260>	3489	294.5
321	G<62>	5568	394.5	371	G<162>	4518	394.5	421	G<262>	3468	394.5
322	G<64>	5547	294.5	372	G<164>	4497	294.5	422	G<264>	3447	294.5
323	G<66>	5526	394.5	373	G<166>	4476	394.5	423	G<266>	3426	394.5
324	G<68>	5505	294.5	374	G<168>	4455	294.5	424	G<268>	3405	294.5
325	G<70>	5484	394.5	375	G<170>	4434	394.5	425	G<270>	3384	394.5
326	G<72>	5463	294.5	376	G<172>	4413	294.5	426	G<272>	3363	294.5
327	G<74>	5442	394.5	377	G<174>	4392	394.5	427	G<274>	3342	394.5
328	G<76>	5421	294.5	378	G<176>	4371	294.5	428	G<276>	3321	294.5
329	G<78>	5400	394.5	379	G<178>	4350	394.5	429	G<278>	3300	394.5
330	G<80>	5379	294.5	380	G<180>	4329	294.5	430	G<280>	3279	294.5
331	G<82>	5358	394.5	381	G<182>	4308	394.5	431	G<282>	3258	394.5
332	G<84>	5337	294.5	382	G<184>	4287	294.5	432	G<284>	3237	294.5
333	G<86>	5316	394.5	383	G<186>	4266	394.5	433	G<286>	3216	394.5
334	G<88>	5295	294.5	384	G<188>	4245	294.5	434	G<288>	3195	294.5
335	G<90>	5274	394.5	385	G<190>	4224	394.5	435	G<290>	3174	394.5
336	G<92>	5253	294.5	386	G<192>	4203	294.5	436	G<292>	3153	294.5
337	G<94>	5232	394.5	387	G<194>	4182	394.5	437	G<294>	3132	394.5
338	G<96>	5211	294.5	388	G<196>	4161	294.5	438	G<296>	3111	294.5
339	G<98>	5190	394.5	389	G<198>	4140	394.5	439	G<298>	3090	394.5
340	G<100>	5169	294.5	390	G<200>	4119	294.5	440	NC	3069	294.5
341	G<102>	5148	394.5	391	G<202>	4098	394.5	441	NC	3048	394.5
342	G<104>	5127	294.5	392	G<204>	4077	294.5	442	NC	3027	294.5
343	G<106>	5106	394.5	393	G<206>	4056	394.5	443	NC	3006	394.5
344	G<108>	5085	294.5	394	G<208>	4035	294.5	444	NC	2985	294.5
345	G<110>	5064	394.5	395	G<210>	4014	394.5	445	NC	2964	394.5
346	G<112>	5043	294.5	396	G<212>	3993	294.5	446	NC	2943	294.5
347	G<114>	5022	394.5	397	G<214>	3972	394.5	447	NC	2835	394.5
348	G<116>	5001	294.5	398	G<216>	3951	294.5	448	NC	2821	294.5
349	G<118>	4980	394.5	399	G<218>	3930	394.5	449	VBD<1>	2807	394.5
350	G<120>	4959	294.5	400	G<220>	3909	294.5	450	S<0>	2793	294.5

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
451	S<1>	2779	394.5	501	S<51>	2079	394.5	551	S<101>	1379	394.5
452	S<2>	2765	294.5	502	S<52>	2065	294.5	552	S<102>	1365	294.5
453	S<3>	2751	394.5	503	S<53>	2051	394.5	553	S<103>	1351	394.5
454	S<4>	2737	294.5	504	S<54>	2037	294.5	554	S<104>	1337	294.5
455	S<5>	2723	394.5	505	S<55>	2023	394.5	555	S<105>	1323	394.5
456	S<6>	2709	294.5	506	S<56>	2009	294.5	556	S<106>	1309	294.5
457	S<7>	2695	394.5	507	S<57>	1995	394.5	557	S<107>	1295	394.5
458	S<8>	2681	294.5	508	S<58>	1981	294.5	558	S<108>	1281	294.5
459	S<9>	2667	394.5	509	S<59>	1967	394.5	559	S<109>	1267	394.5
460	S<10>	2653	294.5	510	S<60>	1953	294.5	560	S<110>	1253	294.5
461	S<11>	2639	394.5	511	S<61>	1939	394.5	561	S<111>	1239	394.5
462	S<12>	2625	294.5	512	S<62>	1925	294.5	562	S<112>	1225	294.5
463	S<13>	2611	394.5	513	S<63>	1911	394.5	563	S<113>	1211	394.5
464	S<14>	2597	294.5	514	S<64>	1897	294.5	564	S<114>	1197	294.5
465	S<15>	2583	394.5	515	S<65>	1883	394.5	565	S<115>	1183	394.5
466	S<16>	2569	294.5	516	S<66>	1869	294.5	566	S<116>	1169	294.5
467	S<17>	2555	394.5	517	S<67>	1855	394.5	567	S<117>	1155	394.5
468	S<18>	2541	294.5	518	S<68>	1841	294.5	568	S<118>	1141	294.5
469	S<19>	2527	394.5	519	S<69>	1827	394.5	569	S<119>	1127	394.5
470	S<20>	2513	294.5	520	S<70>	1813	294.5	570	S<120>	1113	294.5
471	S<21>	2499	394.5	521	S<71>	1799	394.5	571	S<121>	1099	394.5
472	S<22>	2485	294.5	522	S<72>	1785	294.5	572	S<122>	1085	294.5
473	S<23>	2471	394.5	523	S<73>	1771	394.5	573	S<123>	1071	394.5
474	S<24>	2457	294.5	524	S<74>	1757	294.5	574	S<124>	1057	294.5
475	S<25>	2443	394.5	525	S<75>	1743	394.5	575	S<125>	1043	394.5
476	S<26>	2429	294.5	526	S<76>	1729	294.5	576	S<126>	1029	294.5
477	S<27>	2415	394.5	527	S<77>	1715	394.5	577	S<127>	1015	394.5
478	S<28>	2401	294.5	528	S<78>	1701	294.5	578	S<128>	1001	294.5
479	S<29>	2387	394.5	529	S<79>	1687	394.5	579	S<129>	987	394.5
480	S<30>	2373	294.5	530	S<80>	1673	294.5	580	S<130>	973	294.5
481	S<31>	2359	394.5	531	S<81>	1659	394.5	581	S<131>	959	394.5
482	S<32>	2345	294.5	532	S<82>	1645	294.5	582	S<132>	945	294.5
483	S<33>	2331	394.5	533	S<83>	1631	394.5	583	S<133>	931	394.5
484	S<34>	2317	294.5	534	S<84>	1617	294.5	584	S<134>	917	294.5
485	S<35>	2303	394.5	535	S<85>	1603	394.5	585	S<135>	903	394.5
486	S<36>	2289	294.5	536	S<86>	1589	294.5	586	S<136>	889	294.5
487	S<37>	2275	394.5	537	S<87>	1575	394.5	587	S<137>	875	394.5
488	S<38>	2261	294.5	538	S<88>	1561	294.5	588	S<138>	861	294.5
489	S<39>	2247	394.5	539	S<89>	1547	394.5	589	S<139>	847	394.5
490	S<40>	2233	294.5	540	S<90>	1533	294.5	590	S<140>	833	294.5
491	S<41>	2219	394.5	541	S<91>	1519	394.5	591	S<141>	819	394.5
492	S<42>	2205	294.5	542	S<92>	1505	294.5	592	S<142>	805	294.5
493	S<43>	2191	394.5	543	S<93>	1491	394.5	593	S<143>	791	394.5
494	S<44>	2177	294.5	544	S<94>	1477	294.5	594	S<144>	777	294.5
495	S<45>	2163	394.5	545	S<95>	1463	394.5	595	S<145>	763	394.5
496	S<46>	2149	294.5	546	S<96>	1449	294.5	596	S<146>	749	294.5
497	S<47>	2135	394.5	547	S<97>	1435	394.5	597	S<147>	735	394.5
498	S<48>	2121	294.5	548	S<98>	1421	294.5	598	S<148>	721	294.5
499	S<49>	2107	394.5	549	S<99>	1407	394.5	599	S<149>	707	394.5
500	S<50>	2093	294.5	550	S<100>	1393	294.5	600	S<150>	693	294.5

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
601	S<151>	679	394.5	651	S<201>	-21	394.5	701	S<251>	-721	394.5
602	S<152>	665	294.5	652	S<202>	-35	294.5	702	S<252>	-735	294.5
603	S<153>	651	394.5	653	S<203>	-49	394.5	703	S<253>	-749	394.5
604	S<154>	637	294.5	654	S<204>	-63	294.5	704	S<254>	-763	294.5
605	S<155>	623	394.5	655	S<205>	-77	394.5	705	S<255>	-777	394.5
606	S<156>	609	294.5	656	S<206>	-91	294.5	706	S<256>	-791	294.5
607	S<157>	595	394.5	657	S<207>	-105	394.5	707	S<257>	-805	394.5
608	S<158>	581	294.5	658	S<208>	-119	294.5	708	S<258>	-819	294.5
609	S<159>	567	394.5	659	S<209>	-133	394.5	709	S<259>	-833	394.5
610	S<160>	553	294.5	660	S<210>	-147	294.5	710	S<260>	-847	294.5
611	S<161>	539	394.5	661	S<211>	-161	394.5	711	S<261>	-861	394.5
612	S<162>	525	294.5	662	S<212>	-175	294.5	712	S<262>	-875	294.5
613	S<163>	511	394.5	663	S<213>	-189	394.5	713	S<263>	-889	394.5
614	S<164>	497	294.5	664	S<214>	-203	294.5	714	S<264>	-903	294.5
615	S<165>	483	394.5	665	S<215>	-217	394.5	715	S<265>	-917	394.5
616	S<166>	469	294.5	666	S<216>	-231	294.5	716	S<266>	-931	294.5
617	S<167>	455	394.5	667	S<217>	-245	394.5	717	S<267>	-945	394.5
618	S<168>	441	294.5	668	S<218>	-259	294.5	718	S<268>	-959	294.5
619	S<169>	427	394.5	669	S<219>	-273	394.5	719	S<269>	-973	394.5
620	S<170>	413	294.5	670	S<220>	-287	294.5	720	S<270>	-987	294.5
621	S<171>	399	394.5	671	S<221>	-301	394.5	721	S<271>	-1001	394.5
622	S<172>	385	294.5	672	S<222>	-315	294.5	722	S<272>	-1015	294.5
623	S<173>	371	394.5	673	S<223>	-329	394.5	723	S<273>	-1029	394.5
624	S<174>	357	294.5	674	S<224>	-343	294.5	724	S<274>	-1043	294.5
625	S<175>	343	394.5	675	S<225>	-357	394.5	725	S<275>	-1057	394.5
626	S<176>	329	294.5	676	S<226>	-371	294.5	726	S<276>	-1071	294.5
627	S<177>	315	394.5	677	S<227>	-385	394.5	727	S<277>	-1085	394.5
628	S<178>	301	294.5	678	S<228>	-399	294.5	728	S<278>	-1099	294.5
629	S<179>	287	394.5	679	S<229>	-413	394.5	729	S<279>	-1113	394.5
630	S<180>	273	294.5	680	S<230>	-427	294.5	730	S<280>	-1127	294.5
631	S<181>	259	394.5	681	S<231>	-441	394.5	731	S<281>	-1141	394.5
632	S<182>	245	294.5	682	S<232>	-455	294.5	732	S<282>	-1155	294.5
633	S<183>	231	394.5	683	S<233>	-469	394.5	733	S<283>	-1169	394.5
634	S<184>	217	294.5	684	S<234>	-483	294.5	734	S<284>	-1183	294.5
635	S<185>	203	394.5	685	S<235>	-497	394.5	735	S<285>	-1197	394.5
636	S<186>	189	294.5	686	S<236>	-511	294.5	736	S<286>	-1211	294.5
637	S<187>	175	394.5	687	S<237>	-525	394.5	737	S<287>	-1225	394.5
638	S<188>	161	294.5	688	S<238>	-539	294.5	738	S<288>	-1239	294.5
639	S<189>	147	394.5	689	S<239>	-553	394.5	739	S<289>	-1253	394.5
640	S<190>	133	294.5	690	S<240>	-567	294.5	740	S<290>	-1267	294.5
641	S<191>	119	394.5	691	S<241>	-581	394.5	741	S<291>	-1281	394.5
642	S<192>	105	294.5	692	S<242>	-595	294.5	742	S<292>	-1295	294.5
643	S<193>	91	394.5	693	S<243>	-609	394.5	743	S<293>	-1309	394.5
644	S<194>	77	294.5	694	S<244>	-623	294.5	744	S<294>	-1323	294.5
645	S<195>	63	394.5	695	S<245>	-637	394.5	745	S<295>	-1337	394.5
646	S<196>	49	294.5	696	S<246>	-651	294.5	746	S<296>	-1351	294.5
647	S<197>	35	394.5	697	S<247>	-665	394.5	747	S<297>	-1365	394.5
648	S<198>	21	294.5	698	S<248>	-679	294.5	748	S<298>	-1379	294.5
649	S<199>	7	394.5	699	S<249>	-693	394.5	749	S<299>	-1393	394.5
650	S<200>	-7	294.5	700	S<250>	-707	294.5	750	S<300>	-1407	294.5

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
751	S<301>	-1421	394.5	801	S<351>	-2121	394.5	851	NC	-2821	394.5
752	S<302>	-1435	294.5	802	S<352>	-2135	294.5	852	NC	-2835	294.5
753	S<303>	-1449	394.5	803	S<353>	-2149	394.5	853	NC	-2943	394.5
754	S<304>	-1463	294.5	804	S<354>	-2163	294.5	854	NC	-2964	294.5
755	S<305>	-1477	394.5	805	S<355>	-2177	394.5	855	NC	-2985	394.5
756	S<306>	-1491	294.5	806	S<356>	-2191	294.5	856	NC	-3006	294.5
757	S<307>	-1505	394.5	807	S<357>	-2205	394.5	857	NC	-3027	394.5
758	S<308>	-1519	294.5	808	S<358>	-2219	294.5	858	NC	-3048	294.5
759	S<309>	-1533	394.5	809	S<359>	-2233	394.5	859	NC	-3069	394.5
760	S<310>	-1547	294.5	810	S<360>	-2247	294.5	860	G<299>	-3090	294.5
761	S<311>	-1561	394.5	811	S<361>	-2261	394.5	861	G<297>	-3111	394.5
762	S<312>	-1575	294.5	812	S<362>	-2275	294.5	862	G<295>	-3132	294.5
763	S<313>	-1589	394.5	813	S<363>	-2289	394.5	863	G<293>	-3153	394.5
764	S<314>	-1603	294.5	814	S<364>	-2303	294.5	864	G<291>	-3174	294.5
765	S<315>	-1617	394.5	815	S<365>	-2317	394.5	865	G<289>	-3195	394.5
766	S<316>	-1631	294.5	816	S<366>	-2331	294.5	866	G<287>	-3216	294.5
767	S<317>	-1645	394.5	817	S<367>	-2345	394.5	867	G<285>	-3237	394.5
768	S<318>	-1659	294.5	818	S<368>	-2359	294.5	868	G<283>	-3258	294.5
769	S<319>	-1673	394.5	819	S<369>	-2373	394.5	869	G<281>	-3279	394.5
770	S<320>	-1687	294.5	820	S<370>	-2387	294.5	870	G<279>	-3300	294.5
771	S<321>	-1701	394.5	821	S<371>	-2401	394.5	871	G<277>	-3321	394.5
772	S<322>	-1715	294.5	822	S<372>	-2415	294.5	872	G<275>	-3342	294.5
773	S<323>	-1729	394.5	823	S<373>	-2429	394.5	873	G<273>	-3363	394.5
774	S<324>	-1743	294.5	824	S<374>	-2443	294.5	874	G<271>	-3384	294.5
775	S<325>	-1757	394.5	825	S<375>	-2457	394.5	875	G<269>	-3405	394.5
776	S<326>	-1771	294.5	826	S<376>	-2471	294.5	876	G<267>	-3426	294.5
777	S<327>	-1785	394.5	827	S<377>	-2485	394.5	877	G<265>	-3447	394.5
778	S<328>	-1799	294.5	828	S<378>	-2499	294.5	878	G<263>	-3468	294.5
779	S<329>	-1813	394.5	829	S<379>	-2513	394.5	879	G<261>	-3489	394.5
780	S<330>	-1827	294.5	830	S<380>	-2527	294.5	880	G<259>	-3510	294.5
781	S<331>	-1841	394.5	831	S<381>	-2541	394.5	881	G<257>	-3531	394.5
782	S<332>	-1855	294.5	832	S<382>	-2555	294.5	882	G<255>	-3552	294.5
783	S<333>	-1869	394.5	833	S<383>	-2569	394.5	883	G<253>	-3573	394.5
784	S<334>	-1883	294.5	834	S<384>	-2583	294.5	884	G<251>	-3594	294.5
785	S<335>	-1897	394.5	835	S<385>	-2597	394.5	885	G<249>	-3615	394.5
786	S<336>	-1911	294.5	836	S<386>	-2611	294.5	886	G<247>	-3636	294.5
787	S<337>	-1925	394.5	837	S<387>	-2625	394.5	887	G<245>	-3657	394.5
788	S<338>	-1939	294.5	838	S<388>	-2639	294.5	888	G<243>	-3678	294.5
789	S<339>	-1953	394.5	839	S<389>	-2653	394.5	889	G<241>	-3699	394.5
790	S<340>	-1967	294.5	840	S<390>	-2667	294.5	890	G<239>	-3720	294.5
791	S<341>	-1981	394.5	841	S<391>	-2681	394.5	891	G<237>	-3741	394.5
792	S<342>	-1995	294.5	842	S<392>	-2695	294.5	892	G<235>	-3762	294.5
793	S<343>	-2009	394.5	843	S<393>	-2709	394.5	893	G<233>	-3783	394.5
794	S<344>	-2023	294.5	844	S<394>	-2723	294.5	894	G<231>	-3804	294.5
795	S<345>	-2037	394.5	845	S<395>	-2737	394.5	895	G<229>	-3825	394.5
796	S<346>	-2051	294.5	846	S<396>	-2751	294.5	896	G<227>	-3846	294.5
797	S<347>	-2065	394.5	847	S<397>	-2765	394.5	897	G<225>	-3867	394.5
798	S<348>	-2079	294.5	848	S<398>	-2779	294.5	898	G<223>	-3888	294.5
799	S<349>	-2093	394.5	849	S<399>	-2793	394.5	899	G<221>	-3909	394.5
800	S<350>	-2107	294.5	850	VBD<2>	-2807	294.5	900	G<219>	-3930	294.5

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
901	G<217>	-3951	394.5	951	G<117>	-5001	394.5	1001	G<17>	-6051	394.5
902	G<215>	-3972	294.5	952	G<115>	-5022	294.5	1002	G<15>	-6072	294.5
903	G<213>	-3993	394.5	953	G<113>	-5043	394.5	1003	G<13>	-6093	394.5
904	G<211>	-4014	294.5	954	G<111>	-5064	294.5	1004	G<11>	-6114	294.5
905	G<209>	-4035	394.5	955	G<109>	-5085	394.5	1005	G<9>	-6135	394.5
906	G<207>	-4056	294.5	956	G<107>	-5106	294.5	1006	G<7>	-6156	294.5
907	G<205>	-4077	394.5	957	G<105>	-5127	394.5	1007	G<5>	-6177	394.5
908	G<203>	-4098	294.5	958	G<103>	-5148	294.5	1008	G<3>	-6198	294.5
909	G<201>	-4119	394.5	959	G<101>	-5169	394.5	1009	G<1>	-6219	394.5
910	G<199>	-4140	294.5	960	G<99>	-5190	294.5	1010	NC	-6240	294.5
911	G<197>	-4161	394.5	961	G<97>	-5211	394.5	1011	NC	-6261	394.5
912	G<195>	-4182	294.5	962	G<95>	-5232	294.5	1012	NC	-6282	294.5
913	G<193>	-4203	394.5	963	G<93>	-5253	394.5	1013	NC	-6303	394.5
914	G<191>	-4224	294.5	964	G<91>	-5274	294.5	1014	NC	-6324	294.5
915	G<189>	-4245	394.5	965	G<89>	-5295	394.5	1015	NC	-6345	394.5
916	G<187>	-4266	294.5	966	G<87>	-5316	294.5				
917	G<185>	-4287	394.5	967	G<85>	-5337	394.5				
918	G<183>	-4308	294.5	968	G<83>	-5358	294.5				
919	G<181>	-4329	394.5	969	G<81>	-5379	394.5				
920	G<179>	-4350	294.5	970	G<79>	-5400	294.5				
921	G<177>	-4371	394.5	971	G<77>	-5421	394.5				
922	G<175>	-4392	294.5	972	G<75>	-5442	294.5				
923	G<173>	-4413	394.5	973	G<73>	-5463	394.5				
924	G<171>	-4434	294.5	974	G<71>	-5484	294.5				
925	G<169>	-4455	394.5	975	G<69>	-5505	394.5				
926	G<167>	-4476	294.5	976	G<67>	-5526	294.5				
927	G<165>	-4497	394.5	977	G<65>	-5547	394.5				
928	G<163>	-4518	294.5	978	G<63>	-5568	294.5				
929	G<161>	-4539	394.5	979	G<61>	-5589	394.5				
930	G<159>	-4560	294.5	980	G<59>	-5610	294.5				
931	G<157>	-4581	394.5	981	G<57>	-5631	394.5				
932	G<155>	-4602	294.5	982	G<55>	-5652	294.5				
933	G<153>	-4623	394.5	983	G<53>	-5673	394.5				
934	G<151>	-4644	294.5	984	G<51>	-5694	294.5				
935	G<149>	-4665	394.5	985	G<49>	-5715	394.5				
936	G<147>	-4686	294.5	986	G<47>	-5736	294.5				
937	G<145>	-4707	394.5	987	G<45>	-5757	394.5				
938	G<143>	-4728	294.5	988	G<43>	-5778	294.5				
939	G<141>	-4749	394.5	989	G<41>	-5799	394.5				
940	G<139>	-4770	294.5	990	G<39>	-5820	294.5				
941	G<137>	-4791	394.5	991	G<37>	-5841	394.5				
942	G<135>	-4812	294.5	992	G<35>	-5862	294.5				
943	G<133>	-4833	394.5	993	G<33>	-5883	394.5				
944	G<131>	-4854	294.5	994	G<31>	-5904	294.5				
945	G<129>	-4875	394.5	995	G<29>	-5925	394.5				
946	G<127>	-4896	294.5	996	G<27>	-5946	294.5				
947	G<125>	-4917	394.5	997	G<25>	-5967	394.5				
948	G<123>	-4938	294.5	998	G<23>	-5988	294.5				
949	G<121>	-4959	394.5	999	G<21>	-6009	394.5				
950	G<119>	-4980	294.5	1000	G<19>	-6030	294.5				

PAD DESCRIPTION

Power Supply

Name	I/O	Description
VDDIO	Power Supply	IO power
VDD1/2/3/5	Power Supply	Analog power
VDDLI	Power Supply	Digital power
VDDLO	Power Supply	Digital power
VPP	Power Supply	OTP power
VSS1	Power Supply	Digital ground
VSS2/3/5	Power Supply	Analog ground
VSS4	Power Supply	Driver ground
VDH	I/O	Positive source driver Voltage
VDHR	I/O	Positive source driver voltage for Red
VDL	I/O	Negative source driver voltage

Micro-Controller interface

Name	I/O	Description
CL	I/O	Cascade clock, output when MS=H, input when MS=L
BS	I	Bus Selection. Select 3-wire / 4-wire SPI interface. L: 4-wire interface. H: 3-wire interface.(Default)
MS	I	Cascade setting pin. L: Slave chip. H: Master chip.
RESETB	I	Global reset pin. Low: reset.
A0	I	When SPI3 is select A0=H mean writing the command index to IST7158CA1-B A0=L mean writing command data or display data to IST7158CA1-B
BUSY_N	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.
CSB	I	Serial communication chip select.
SDA	I/O	Serial communication data input/output
SCL	I	Serial communication clock input.
TSCL	I/O	Cascade line sync, output when MS=H, input when MS=L
TSDA	I/O	Cascade frame sync, output when MS=H, input when MS=L
CPBI	O	Check Panel broken input singal
CPBO	O	Check Panel broken output signal
GDR	O	N-MOS gate control, for booster circuit output.
RESE	O	Current sense input for control loop.
FB	O	(Keep Open.)
NC	-	Not Connected.

LCD Driver outputs

Name	I/O	Description
S<399:0>	O	Source driver output signals.
VBD<2:1>	O	Border output pins.
G<299:0>	O	Gate driver output signals.
VGH	I/O	Positive Gate voltage.
VGL	I/O	Negative Gate voltage.
VCOM	O	VCOM output.

I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
VDDIO,VDD1/2/3/5,VSS1/2/3/4/5,VDDLI,VDDLO	<10Ω
VGH,VGL,VDH,VCOM,VDL,VDHR	<5Ω
VPP	<10Ω
BS,MS,BUSY_N,CSB,SDA,SCL,TSCL,TSDA,CL A0,CPBI,CPBO, GDR,RESE,FB	<1KΩ
RESETB	<10KΩ

FUNCTIONAL DESCRIPTION

Microprocessor Interface

CSB pin is used for chip selection. The IST7158CA1-B can interface with an MPU only when CSB is "L". When these pins are set to any other combination, A0, SCL, inputs are disabled and SDA are high impedance. In case of serial interface, the internal shift registers and the counter are reset.

MPU Interface types

IST7158CA1-B has two types of MPU interface, which are two serial interfaces, SPI3 and SPI4 serial interface is determined by BS pin as shown below.

BS	Type	Interface mode
H	SPI3	3-Line SPI Serial-mode
L	SPI4	4-Line SPI Serial-mode

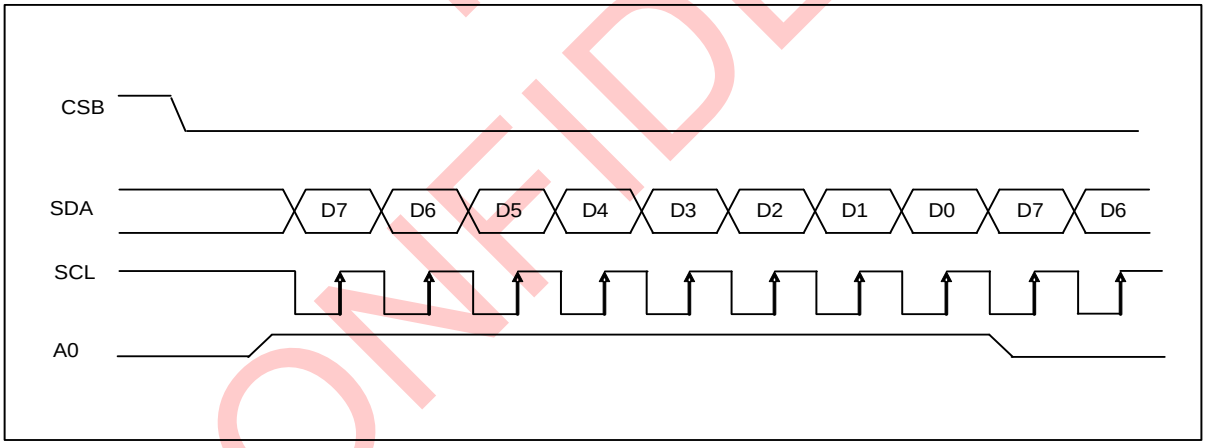
4-wire Serial Interface (BS= "L")

When BS= "L", the IST7158CA1-B configured as Serial interface(4-line), the serial data can be input/output through SDA and serial clock can be input through SCL.

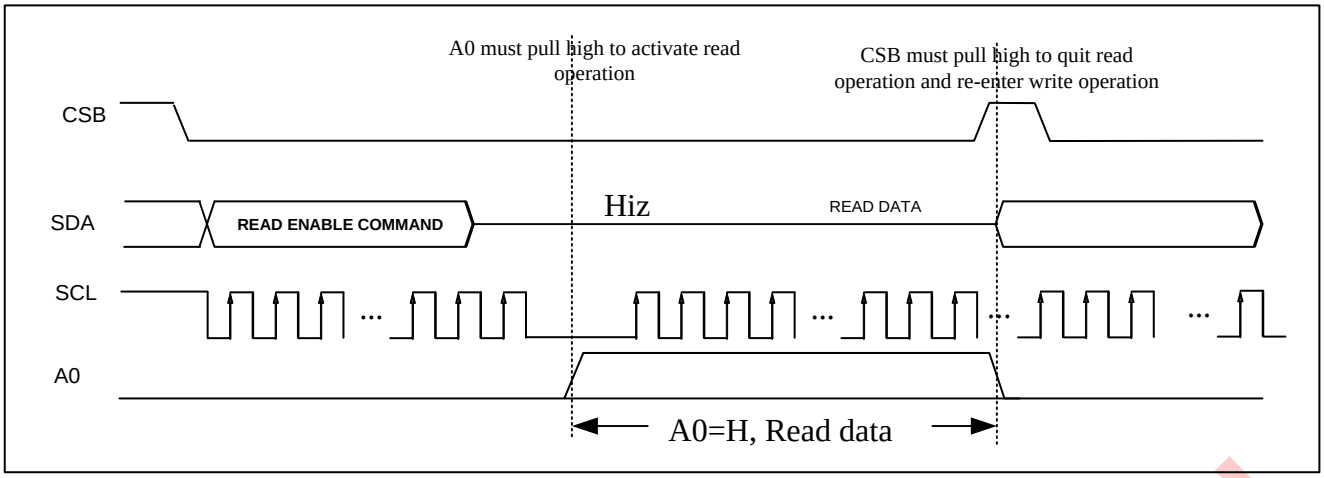
When the chip is not selected, the shift register & serial data counter will be reset and SDA & SCL will also be disabled internally.

When the chip is selected (CSB="L"), the serial data can be shifted in sequentially at the rising edge of SCL and transferred to 8-bit parallel data internally; at the eighth SCL rising edge, A0 will also be sampled to decide these 8-bit data is interpreted as command or display data.

4-Line Serial Interface Timing



Write operation of 4-Line SPI



Read operation of 4-Line SPI

Note:

1. After read enable command is set, SDA must set Hiz, and A0 set high to activate read operation
2. When read operation is done, CSB must set high once to quit read operation.

3-wire Serial Interface (BS= "H")

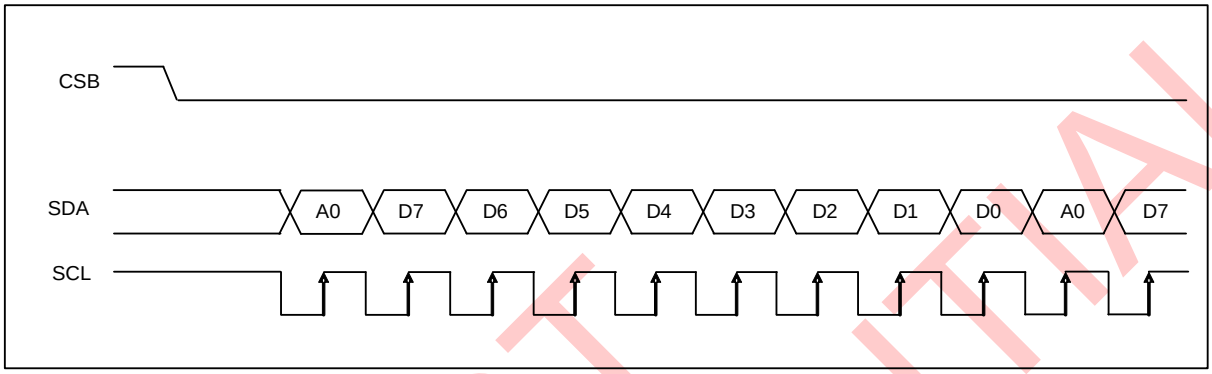
When BS= "H", the IST7158CA1-B configured as Serial interface(3-line), the serial data can be input/output through SDA and serial clock can be input through SCL.

When the chip is not selected, the shift register & serial data counter will be reset and SDA&SCL will also be disabled internally.

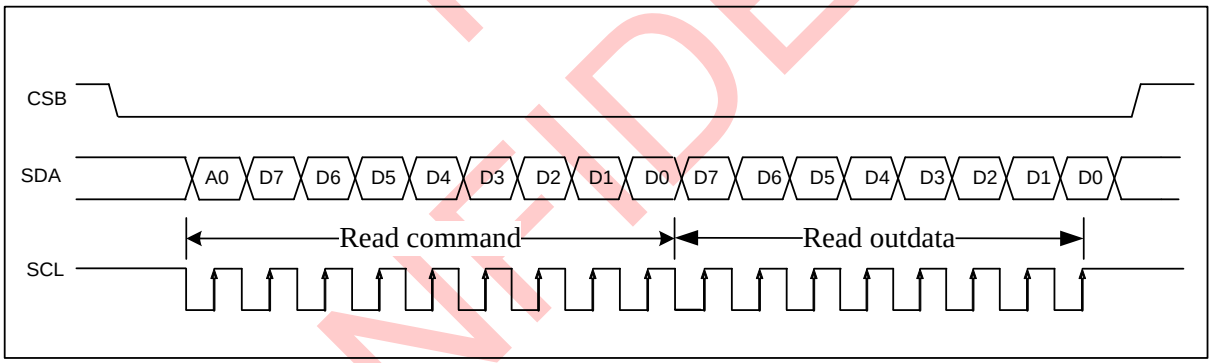
In 3-Line interface, A0 signal is not available and the 1st output of SDA will be treated as A0 flag.

When the chip is selected (CSB="L"), when1th SCL rising edge arise, SDA will be sampled as A0, 2th~9th SCL rising edge will shift the SDA to be a 8bit parallel data. and A0 will deside the 8bit data as command index or command dataor display data.

3-LineSerial Interface Timing



Write operation of 3-Line SPI



Read operation of 3-Line SPI

Busy Flag

The Busy Flag indicates whether the IST7158CA1-B is still during operation or not. When BUSY is "L", IST7158CA1-B is busy, and customer can read status from IST7158CA1-B to find out which operation trige the BUSY singal, It is not recommand writing display data or other command to IST7158CA1-B, except read the status of IST7158CA1-B.

COMMAND DESCRIPTION

R00H(PSR): Panel setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PSR	W	0	0	0	0	0	0	0	0	0	(00H)
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	1	(0FH)
2nd Parameter	W	1	LUT_EN	0	FOPT	VCMZ	1	TIEG	NORG	VC_LUTZ	(09H)

1st Parameter:

Bit7-6	Resolution setting
00b	Display resolution is 400x300 (default)
01b	Display resolution is 300x300
10b	Display resolution is 256x256
11b	Display resolution is 128x128

Bit5	Power switch operation mode
0	Power switching time in the period of frame scanning.(default).
1	Power switching time in the external period before frame scanning.

Bit3	UD function(*1)
0	Scandown; First line=Gn,Gn-1, … G2, Last line=G1
1	Scanup; First line=G1,G2, … ,Gn-1, Last line=Gn.(default)

Bit2	SHL function(*2)
0	Shift left; First data=Sn,Sn-1, … ,S2, Last data=S1.
1	Shift right; First data=S1,S2, … ,Sn-1, Last data=Sn.(default)

Bit1	SHD_N function(*3)
0	Booster OFF, register data are kept,and Source/Border/VCOM are kept 0V or floating
1	Booster ON.(default)

2nd Parameter:

Bit0	VC_LUTZ function
0	NO effect.
1	After refreshing display,the output of VCOM is set to floating automatically(default)

Bit1	NORG function
0	NO effect.(default)
1	After refreshing display,VCOM is tied to GND before power off

Bit2	TIEG function
0	NO effect.(default)
1	After power off booster,VGL will be tied to GND.

Bit4	VCMZ function
0	NO effect.(default)
1	VCOM is always floating.

Bit5	FOPT function
0	Scan 1 frame after waveform finished (Default)
1	No Scan after waveform finished and switch the source channel output to HiZ

Bit7	LUT_EN
0	LUT from OTP(default)
1	LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.

FOPT: Power off floating.

Notes:

1. Non-select gate line keep at VGL for DSP/DRF and AMV
2. Inactive source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R01H(PWR): Power Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWR	W	0	0	0	0	0	0	0	0	1	(01H)
1st Parameter	W	1	-	-	-	-	V_MODE	VSC_EN	VS_EN	VG_EN	(07H)
2nd Parameter	W	1	-	-	-	-	-	-	VG[1]	VG[0]	(00H)
3rd Parameter	W	1	-	VDHR [6]	VDHR [5]	VDHR [4]	VDHR [3]	VDHR [2]	VDHR [1]	VDHR [0]	(00H)
4th Parameter	W	1	-	VDH [6]	VDH [5]	VDH [4]	VDH [3]	VDH [2]	VDH [1]	VDH [0]	(00H)
5th Parameter	W	1		VDL[6]	VDL [5]	VDL [4]	VDL [3]	VDL [2]	VDL [1]	VDL [0]	(00H)
6th Parameter	W	1		VDHR1 [6]	VDHR1 [5]	VDHR1 [4]	VDHR1 [3]	VDHR1 [2]	VDHR1 [1]	VDHR1 [0]	(00H)

Power mode switch mapping:

Mode 0 : 0V & +15V & -15V & VDHR (+3V~+15V)

Mode 1 : 0V & VDH (+3V~+15V) & VDL (-3V~-15V) & VDHR1 (+3V~+15V)

1st Parameter:

Bit3	Initial source power mode.
0	Mode0. (default)
1	Mode1.

Bit2	Source LV power selection.
0	External source LV power from VDHR pins.
1	Internal DC/DC function for generate VDHR.

Bit1	Source power selection.
0	External source power from VDH/VDL pins.
1	Internal DC/DC function for generate VDH/VDL.

Bit0	Gate power selection.
0	External gate power from VGH/VGL pins.
1	Internal DCDC function for generate VGH/VGL.

2nd Parameter:

Bit1-0	VGH & VGL Voltage Level.
00	VGH=20v, VGL=-20v(default)
01	VGH=17v, VGL=-17v
10	VGH=15v, VGL=-15v
11	VGH=10v, VGL=-10v

3rd & 4th Parameter: Internal VDHR/VDH power selection (Default value: 0000000b)

5th & 6th Parameter: Internal VDL/VDHR1 power selection (Default value: 0000000b)

Bit6-0	Internal VDH selection.	Internal VDL selection.	Bit6-0	Internal VDH selection.	Internal VDL selection.
0000000	3V	-3V	0110010	8.0V	-8.0V
0000001	3.1V	-3.1V	…	…	…
0000010	3.2V	-3.2V	0111100	9.0V	-9.0V
0000011	3.3V	-3.3V	…	…	…
0000100	3.4V	-3.4V	1000110	10.0V	-10.0V
0000101	3.5V	-3.5V	…	…	…
0000110	3.6V	-3.6V	1010000	11.0V	-11.0V
0000111	3.7V	-3.7V	…	…	…
0001000	3.8V	-3.8V	1011010	12.0V	-12.0V
0001001	3.9V	-3.9V	…	…	…
0001010	4.0V	-4.0V	1100100	13.0V	-13.0V
0001011	4.1V	-4.1V	…	…	…
0001100	4.2V	-4.2V	1101110	14.0V	-14.0V
0001101	4.3V	-4.3V	…	…	…
0001110	4.4V	-4.4V	1111000	15.0V	-15.0V
0001111	4.5V	-4.5V			
0010000	4.6V	-4.6V			
…	…	…			
0010100	5.0V	-5.0V			
…	…	…			
0011110	6.0V	-6.0V			
…	…	…			
0101000	7.0V	-7.0V			
…	…	…			

Notes:

1. If gate voltage is set to +/-17v, +/-15v, +/-10v, IC will auto correct source voltage as follows:
2. VGH-VDH/VDH/VDHR1 ≧ 2v
3. VGL-VDL ≧ -2v

R02H(POF): Power OFF Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
POF	W	0	0	0	0	0	0	0	1	0	(02H)
1st Parameter	W	1	-	-	-	-	-	-	-	EDSE	(00H)

After power off command, driver will power off base on power off sequence. After power off command, BUSY_N signal will become "0".

Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register will keep until VDD become off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R03H(POFS): Power on/off Sequence Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PFS	W	0	0	0	0	0	0	0	1	1	(03H)
1st Parameter	W	1	-	-	T_VDPG_OFF		-	-	T_VDS_OFF		(00H)

1st Parameter:

Bit1-0	Power off sequence of VDH and VDL
00b	20ms(default)
01b	40ms
10b	60ms
11b	80ms

Bit5-4	Power off sequence of VGH and VGL
00b	20ms(default)
01b	40ms
10b	60ms
11b	80ms

R04H(PON):Power ON Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PON	W	0	0	0	0	0	0	1	0	0	(04H)

After power on command, the driver will power ON base on Power ON sequence.

After power on command and all power sequence are ready (based on PWR command), then BUSY_N signal will become “1”.

This command only active when BUSY_N=“1”.

R06H(BTST): Booster Soft Command Reglster

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LUT0	W	0	0	0	0	0	0	1	1	0	(06H)
1st Parameter	W	1	**BT_PHA1**	**BT_PHA0**	0	0	0	0	0	0	(00H)
2st Parameter	W	1	**BT_PHB1**	**BT_PHB0**	0	0	0	0	0	0	(00H)
3st Parameter	W	1	**BT_PHC1**	**BT_PHC0**	0	0	0	0	0	0	(00H)

Control of Power On time.

D7-D6	BT_PHA/B/C perild
00	10ms (default)
01	20ms
10	30ms
11	40ms

R07H(DSLP): Deep Sleep Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSLP	W	0	0	0	0	0	0	1	1	1	(07H)
1st Parameter	W	1	1	0	1	0	0	1	0	1	(A5H)

After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excited if check code = 0xA5.

R10H(DTM): Data Start Transmission Register

`	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DTM	W	0	0	0	0	1	0	0	0	0	(10H)
2-bit mode											
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		(00H)
⋮	W	1	: :		: :		: :		: :		(00H)
Nth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		(00H)

NOTE:"-" Don't care, can be set to VDD or GND level. "X": Dummy data, it would not be stored in frame buffer.

This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data for panel.

Pixel[1~n][1:0](2-bit mode):

`	Source Driver Output			
ImageData	DDX=1(Default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00	Gray0	ogray00	Gray3	ogray03
01	Gray1	ogray01	Gray2	ogray02
10	Gray2	ogray02	Gray1	ogray01
11	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1, Pixel[1:0]=01 -> Gray level select = Gray1, follow LUT data output from IP output port "ogray01".
When DDX=0, Pixel[1:0] = 11 -> Gray level select = Gray 0, follow LUT data output from IP output port "ogray00".

R11H(DSP): DataStop Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSP	W	0	0	0	0	1	0	0	0	1	(11H)
1st Parameter	R	1	data_flag	-	-	-	-	-	-	-	(00H)

To stop data transmission,this command must be issued to check the data_flag.

1st Parameter:

Bit7	Data flag of receiving user data.
0	Driver didn't receive all the data.
1	Driver has already received all the one frame data.

After "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.

This command only active when BUSY_N = "1".

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R12H(DRF): Display Refresh Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DRF	W	0	0	0	0	1	0	0	1	0	(12H)
1st Parameter	W	1	-	-	-	-	-	-	-	AC/DCVCOM	(00H)

While user sent this command,driver will refresh display(data/VCOM) base on SRAM data and LUT.

AC/DCVCOM: AC,DC VCOM select.

0: ACVCOM,VCOM will follow LUTC when updating image. (default)

1: DCVCOM,VCOM will always be VCOMDC when updating image

After display refresh command, BUSY_N signal will become “0”

This command only active when BUSY_N = “1”.

R17H(AUTO): Auto Sequence Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Auto Sequence	W	0	0	0	0	1	0	1	1	1	(17H)
	W	1	1	0	1	0	0	1	0	1	(A5H)

The command can enable the internal sequence to execute several commands continuously.

The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO(0x17)+Code(0xA5)=(PON → DRF → POF)

AUTO(0x17)+Code(0xA7)=(PON → DRF→ POF → DSLP)

R20H(LUT0): LUT0 Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LUT0	W	0	0	0	1	0	0	0	0	0	(20H)
1st Parameter	W	1	Data 0								(00H)
.....		1	.....								(00H)
535th Parameter	W	1	Data 534								(00H)

Write LUT0 register from MCU interface

R30H(PLL): PLL Control Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PLL	W	0	0	0	1	1	0	0	0	0	(30H)
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	(02H)

The command controls the PLL clock frequency.The PLL structure must support the following frame rates:

Bit3	Dynamic frame rate (EInk use only)
0	Disable(default)
1	Enable

FR[2:0]	Framerate
000	12.5 Hz
001	25 Hz
010	50 Hz (default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

R40H(TSC): Temperature Sensor Command Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	0	0	0	0	0	0	(40H)
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	(00H)

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads temperature sensor value.

BUSY_N become low after TSC command. When BUSY_N become high, Parameter can be read.
This command only active when BUSY_N="1"

Temperature boundary: -25C~60C

TS[7:0]/D[10:3]	Temperature (°C)	TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25	0000_0000	0
1110_1000	-24	0000_0001	1
1110_1001	-23	0000_0010	2
1110_1010	-22	0000_0011	3
1110_1011	-21	0000_0100	4
1110_1100	-20	0000_0101	5
1110_1101	-19	0000_0110	6
…	…	…	…
1111_1110	-2	0011_1011	59
1111_1111	-1	0011_1100	60

R41H(TSE): Temperature Sensor Enable Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSE	W	0	0	1	0	0	0	0	0	1	(41H)
1st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	(00H)

This command indicates the driver IC temperature sensor enable and calibration function.

1st Parameter:

Bit7	Internal temperature sensor enable
0	Enable internal temperature sensor. (default)
1	Disable internal temperature sensor, using external temperature sensor.

Bit3-0	Temperature level	Bit3-0	Temperature level
0000	+0℃(Default)	1000	-4℃
0001	+0.5℃	1001	-3.5℃
…	…	…	…
0111	+3.5℃	1111	-0.5℃

Bit[3:0]: Reserve one temperature offset TO[3:0] for calibration

1. TO[3]: mean ”+” or ”-“ while 0 is “+”; 1 is ”-“

2. TO[2:0]: mean temperature offset value

R44H(GPI Sensing): GPIO Input Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Check Panel Glass	W	0	0	1	0	0	0	1	0	0	(44H)
	W	1	-	-	-	-	-	-	-	GPIS	(00H)

This command will indicate status of GPI

GPIS : 0 detected low logic on GPIO

1 detected high logic on GPIO

R50H(CDI): VCOM and DATA Interval Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CDI	W	0	0	1	0	1	0	0	0	0	(50H)
1st Parameter	W	1	VBD[2]	VBD[1]	VBD[0]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	(97H)

This command can set 2 kinds of parameters,1.VCOM to data output interval(CDI) 2.Border pin output.

VBD[2:0]: Border data selection (from LUT output by IP port border_w[1:0]).

This register will make border pin output being mapped to a certain grayscale.

DDX[0]	VBD[2:0]	Gray level select	IP setting for Border LUT select
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (Default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating(Default)	N/A

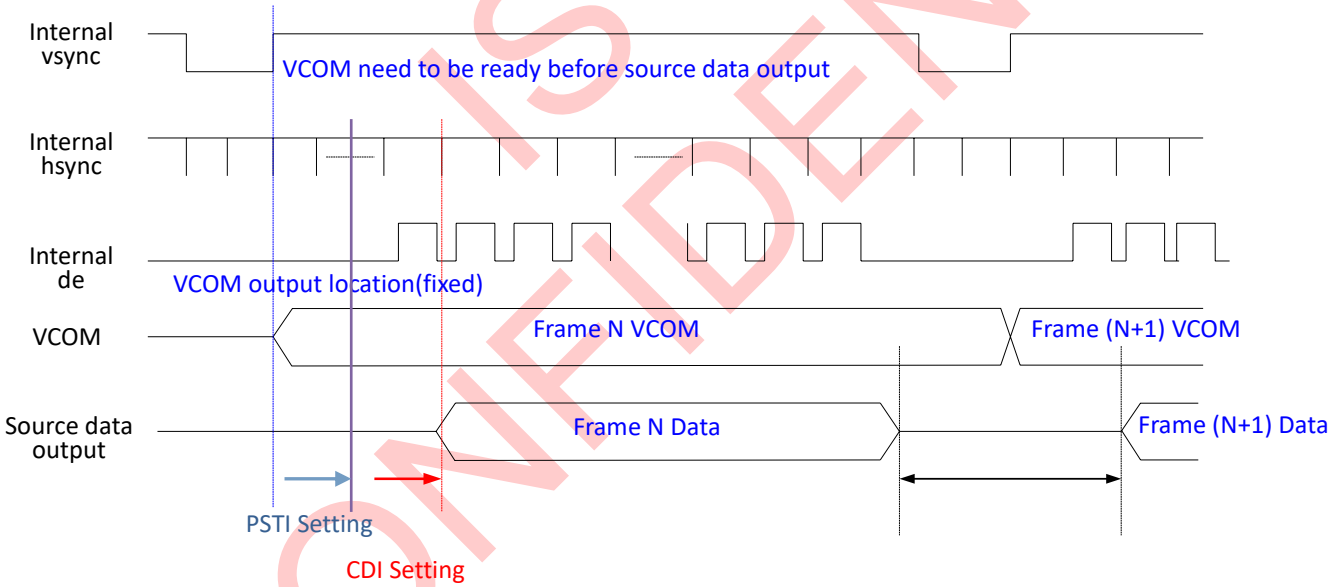
Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V, without VCOM offset,the real output on Border pin shall be 15V+VCOMDC.

Border output will follow FOPT definition being defined in R00h

This command indicates the interval of Vcom and data output.When setting the vertical backporch, the total blanking will be kept as a default value (count by HSYNC)

Bit3	Bit2	Bit1	Bit0	VCOM and data interval
0	0	0	0	17 hsync
0	0	0	1	16 hsync
0	0	1	0	15 hsync
0	0	1	1	14 hsync
0	1	0	0	13 hsync
0	1	0	1	12 hsync
0	1	1	0	11 hsync
0	1	1	1	10 hsync (Default)
1	0	0	0	9 hsync.
1	0	0	1	8 hsync
1	0	1	0	7 hsync
1	0	1	1	6 hsync
1	1	0	0	5 hsync
1	1	0	1	4 hsync
1	1	1	0	3 hsync
1	1	1	1	2 hsync



R51H(LPD): Lower Power Detection Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LPD	W	0	0	1	0	1	0	0	0	1	(51H)
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	(01H)

This command indicates the input power condition. Host can read this data to understand the battery condition.

When LPD="1",system input power is normal.

When LPD="0",Low power input (VDD<2.5V,selected by LVD_SEL[1:0] in command LVSEL)

Bit0	LPD
0	Lowpowerinput.
1	Normalstatus.(Default)

This command only active when BUSY_N="1".

R60H (TCON): TCON setting Register

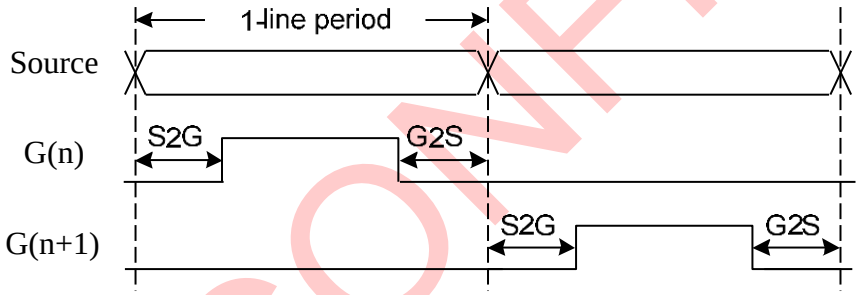
Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	1	0	0	0	0	0	(60H)
1st Parameter	W	1	-	-	S2G[5]	S2G[4]	S2G[3]	S2G[2]	S2G[1]	S2G[0]	(02H)
2nd Parameter	W	1	-	-	G2S[5]	G2S[4]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	(02H)

The command define as Non-overlap period of gate and source and as below:

S2G[5:0] or G2S[5:0]	Period
0	1unit
1	2unit
2	3unit(Default)
3	4unit
4	5unit
5	6unit
6	7unit
7	8unit
8	9unit
9	10unit
10	12unit
11	14unit
12	16unit
13	18unit
….	…
63	118unit

1 unit = 500ns

Gon_T= 1 line period – S2G –G2S, minimum Gon_T = 2 units. If(1line period – S2G –G2S) <2 units , Gon_T = 2 units



R61H(TRES): Resolution Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TRES	W	0	0	1	1	0	0	0	0	1	(61H)
1st Parameter	W	1	0	0	0	0	0	0	0	HRES(8)	(00H)
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	(00H)
3rd Parameter	W	1	0	0	0	0	0	0	0	VRES(8)	(00H)
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	(00H)

Note: HRES ≦ Horizontal line of PSR, VRES ≦ Vertical line of PSR.

No matter what value being set in D1 and D0 of 1st parameter(HRES[1] and HRES[0]), the register shall be kept as 0

When using register:

Horizontal display resolution = HRES

Vertical display resolution = VRES

Channel disable calculation:

GD: First G active=G0; LAST active GD = first active+VRES[8:0]-1

SD: First active channel:=S0; LAST activeSD = first active+HRES[8:2]*4-1

R65H(GSST): GATE/SOURCE START SETTING

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GSST	W	0	0	1	1	0	0	1	0	1	(65H)
1st Parameter	W	1	0	0	0	0	0	0	0	HST (8)	(00H)
2nd Parameter	W	1	HST (7)	HST (6)	HST (5)	HST (4)	HST (3)	HST (2)	0	0	(00H)
3rd Parameter	W	1	0	0	0	0	0	0	0	VST (8)	(00H)
4th Parameter	W	1	VST (7)	VST (6)	VST (5)	VST (4)	VST (3)	VST (2)	VST (1)	VST (0)	(00H)

This command defines resolution start gate/source position.

HST[8:2]: Horizontal Display Start Position (Source)

VST[8:0]:Vertical Display Start Position (Gate)

R70H(REV): Chip Revision Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
REV	W	0	0	1	1	1	0	0	0	0	(70H)
1st Parameter	R	1	REV0[7]	REV0[6]	REV0[5]	REV0[4]	REV0[3]	REV0[2]	REV0[1]	REV0[0]	(06H)
2nd Parameter	R	1	REV1[7]	REV1[6]	REV1[5]	REV1[4]	REV1[3]	REV1[2]	REV1[1]	REV1[0]	(04H)
3rd Parameter	R	1	REV2[7]	REV2[6]	REV2[5]	REV2[4]	REV2[3]	REV2[2]	REV2[1]	REV2[0]	(01H)

1nd Parameter:

Bit7-0	REV0
-	EInk internal number

2nd Parameter:

Bit7-0	REV1
-	EInk internal number

3rd Parameter:

Bit7-0	REV2
-	Increased each revision

R80H(AMV): Auto Measurement VCOM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
AMV	W	0	1	0	0	0	0	0	0	0	(80H)
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	AMVX	AMVS	AMV	AMVE	(00H)

This command indicates the IC status.Host can read this data to understand the IC status.

This command only active when BUSY_N="1"

1st Parameter:

Bit7-6	The sensing points of sampling time
00	2(default)
01	4
10	8
11	16

Sampling time= the last quarter of sensing time (T)

VCOM = average of N points. N=2,4,8,16

Bit5-4	The sensing time of VCOM detection
00	5s(default)
01	10s
10	15s
11	20s

Bit3	XON setting for all Gate ON of AMV
0	Gate scan normally during Auto Measure VCOM period.(default)
1	All Gate ON during Auto Measure VCOM period.

Bit2	AMVS setting for Source output of AMV
0	Source output 0V during Auto Measure VCOM period.(default)
1	Source output VSPL during Auto MeasureVCOM period.

Bit1	Analogy signal
0	Get VCOM value by R81H(default)
1	Gate scan only. Measure VCOM externally by probing the VCOM pad.

Bit0	Auto Measure VCOM setting
0	Auto measure VCOM disble (default)
1	Auto measure VCOM enable

R81H(VV): VCOM Value Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VV	W	0	1	0	0	0	0	0	0	1	(81H)
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	(00H)

This command gets Vcom value.

1st Parameter:

Bit6-0	VCOM value
0000000	0V
0000001	-0.05V
0000010	-0.10V
⋮	⋮
1010000	-4.00V
Others	-

R82H(VDCS): VCM_DC Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VDCS	W	0	1	0	0	0	0	0	1	0	(82H)
1st Parameter	W	1	OTP_VCM	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	(00H)

This command set the VCOMDC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit7	Follow OTP VCOM value in OTP mode
0	IP output value(default)
1	From the setting register

Bit6-0	VCOM value
0000000	0V(default)
0000001	-0.05V
0000010	-0.10V
⋮	⋮
1010000	-4.00V
Others	-

R90H(PGM): Program Mode

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Ente rProgram Mode	W	0	1	0	0	1	0	0	0	0	(90H)

After this command is issued,the chip would enter the program mode.

After the programming procedure completed,a hardware reset is necessary for leaving program mode

R91H(APG): Active Program

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Active Program OTP	W	0	1	0	0	1	0	0	0	1	(91H)

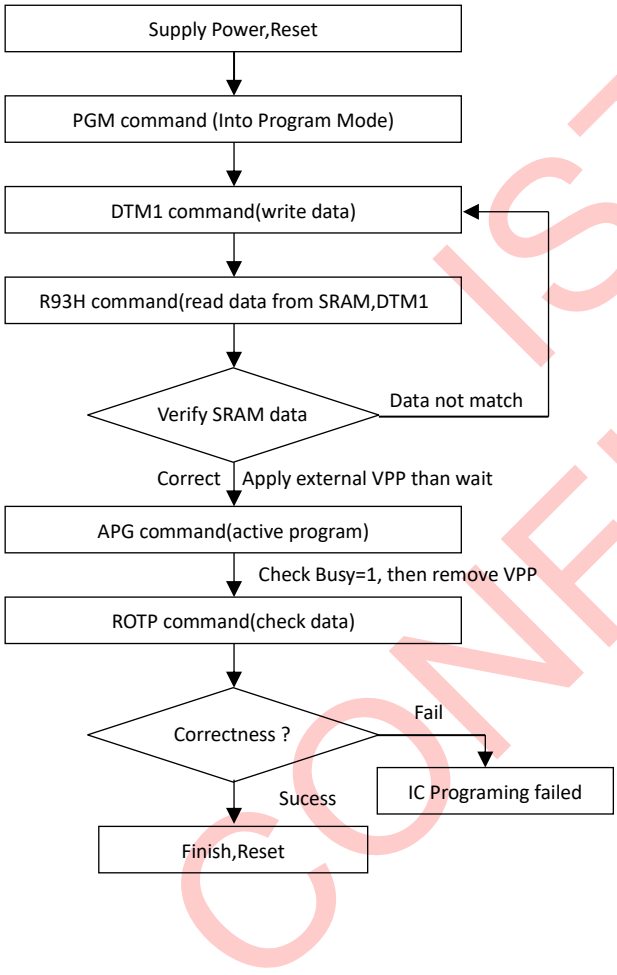
After this command is transmitted,the programming state machine would be activated.

The BUSY_N flag would fall to 0 until the programming is completed.

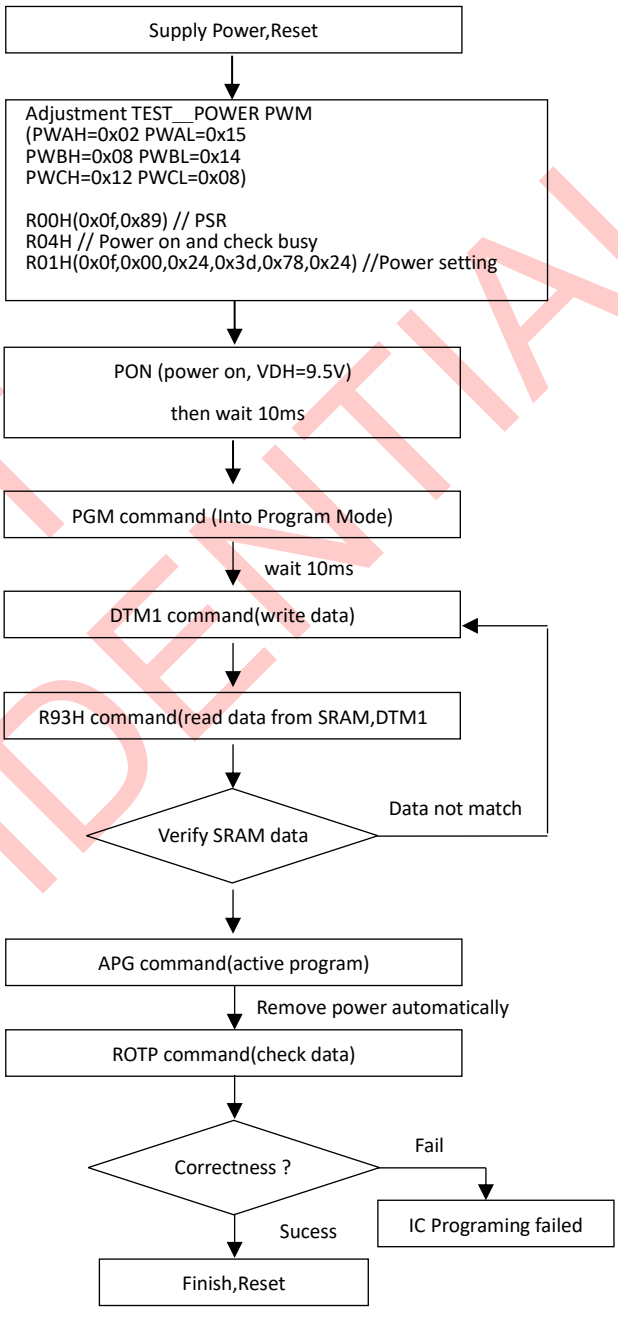
This command only active when BUSY_N="1"

R92H(ROTP): Read OTP Data

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read OTP Data	W	0	1	0	0	1	0	0	1	0	(92H)
	R	1	Dummy								(00H)
	R	1	The data of address0 in the OTP								(00H)
	R	1									(00H)
	R	1	The data of address(n) in the OTP								(00H)



OTP Programming Flow (External VPP)



OTP Programming Flow (Internal VPP)

R93H(RSRAM):Read SRAM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read SRAM Data	W	0	1	0	0	1	0	0	1	1	(93H)
	R	1	Dummy								(00H)
	R	1	The data of address0 in the SRAM								(00H)
	R	1									(00H)
	R	1	The data of address(n) in the SRAM								(00H)

RA2H(PGM_CFG):OTP Program Config Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP program Config	W	0	1	0	1	0	0	0	1	0	(A2H)
1st Parameter	W	1	-	-	-	VPPSEL	-	-	**M_dis**	**S_dis**	(00H)
2nd Parameter	W	1	PGM_SADDR[15:8]								(00H)
3rd Parameter	W	1	PGM_SADDR[7:0]								(00H)
4th Parameter	W	1	PGM_DSIZE[15:8]								(15H)
5th Parameter	W	1	PGM_DSIZE[7:0]								(DFH)

This command is to set the configuration of OTP

1st Parameter

Bit4	VPPSEL
0	External VPP **(default)**
1	Internal VPP

Bit1	M_dis
0	Enable specific command **(default)**
1	Disable specific command

Enable/Disable some command when IC sets Master (MS Pin is High).

Bit0	S_dis
0	Enable specific command **(default)**
1	Disable specific command

Enable/Disable some command when IC sets Slave (MS Pin is Low).

***Notes: Specific command define: R00H(Parameter 1)(PSR), R10H(DTM), R90H(PGM), R91H(APG)**

***For command reading, only the bit of M_dis or S_dis can be set to 1.**

2nd and 3rd Parameters: Program start address PGM_SADDR[15:0]

4th and 5th Parameters: Program data size PGM_SADDR[15:0]

Default PGM_DSIZE[15:0] is 0x15DF.

RA3H(PGM_STAT):OTP Program Status Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP program Status	W	0	1	0	1	0	0	0	1	1	(A3H)
1st Parameter	W	1	-	-	-	-	-	-	PGM_VER_ERR	PGM_EXE_ERR	(00H)

This command is to read OTP Program status

1st Parameter:

Bit1	Data verification of APG
0	OK
1	NOK

Bit0	OTP program execution status
0	Normal
1	Invalid APG setting

RE0H(CCSET):Chip Temperature Input Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Temperature Input	W	0	1	1	1	0	0	0	0	0	(E0H)
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	**CCEN**	(00H)

This command is control input path of temperature value

1st Parameter:

Bit0	Output clock enable/disable
0	Output 0v at CL pin **(default)**
1	Ouptut clock at CL pin for alave chip.(**Cascade mode**)

CCEN=1 : The master temperature is synchronized with the salve. The MCU should delay about 1ms.

Bit1	Temperature Input Selection
0	Use temperature sensor **(default)**
1	Use TSSET[7:0] value

RE4H(LVSEL): LVD Voltage Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Select LVD Voltage	W	0	1	1	1	0	0	1	0	0	(E4H)
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		(03H)

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVDvalue
00	<2.2V
01	<2.3V
10	<2.4V
11	<2.5V (default)

RE6H(TSSET): Force Temperature Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Force Temperature	W	0	1	1	1	0	0	1	1	0	(E6H)
1st Parameter	W	1	TS[7]	TS[6]	TS[5]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]	(00H)

TS[7:0]: Temperature boundary: -25C~60C

When TSFIX=1, Internal TS is disable, Temperature value will be set by TS[7:0].

TS[7:0]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
…	…
1111_1110	-2
1111_1111	-1

TS[7:0]	Temperature (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
…	…
0011_1011	59
0011_1100	60

RFFH(TEST): Enter TEST MODE

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	1	1	(FFH)
1st Parameter	W	1	1	0	1	0	0	1	0	1	(A5H)

TEST(0xFF)+Code(0xA5)=Enter TEST MODE

RFFH(TEST): Exit TEST MODE

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	1	1	(FFH)
1st Parameter	W	1	1	1	1	0	0	0	1	1	(E3H)

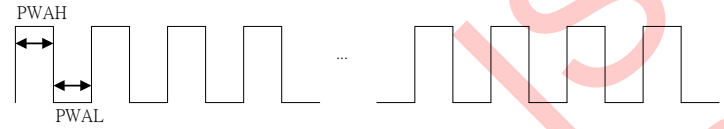
TEST(0xFF)+Code(0xE3)=Exit TEST MODE

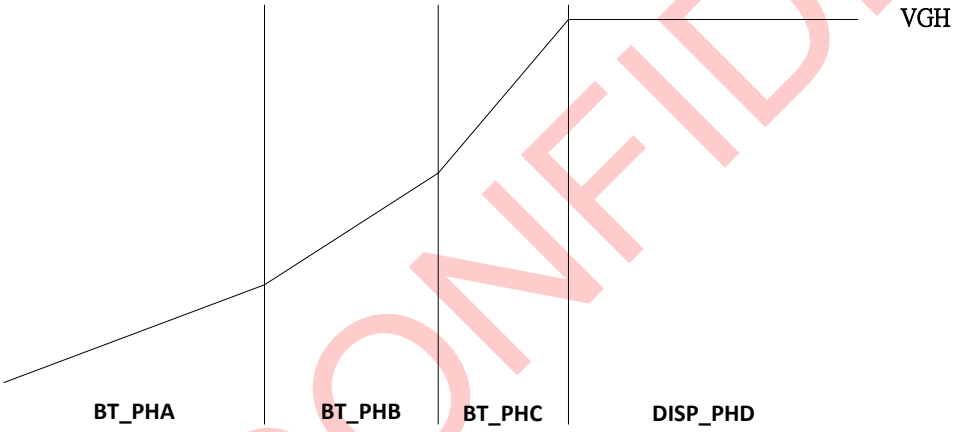
REFH(TEST): POWER PWM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	1	1	1	(EFH)
1st Parameter	W	1	BT_PWAH								(01H)
2st Parameter	W	1	BT_PWAL								(03H)
3st Parameter	W	1	BT_PWBH								(03H)
4st Parameter	W	1	BT_PWBL								(0AH)
5st Parameter	W	1	BT_PWCH								(04H)
6st Parameter	W	1	BT_PWCL								(20H)
7st Parameter	W	1	DISP_PWDH								(06H)
8st Parameter	W	1	DISP_PWDL								(20H)

1nd Parameter:

Bit7-0	PWxH/L time
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns





1st、2nd parameter : correspond to the PWM duty cycle within a specified time for the R06H command BT_PHA.

3rd、4th parameter : correspond to the PWM duty cycle within a specified time for the R06H command BT_PHB.

5th、6th parameter : correspond to the PWM duty cycle within a specified time for the R06H command BT_PHC.

7th、8th parameter : the PWM duty cycle within display refresh(DISP_PHD).

RC9H(TEST): GDROTP

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	0	1	0	0	1	(C9H)
1st Parameter	W	1	GDR_OTP_R								(F8H)

Adjust the GDR driving for the three-stage voltage boosting during POWER ON and display refresh.

Bit7-6	GDR driving within DISP_PHD
Bit5-4	GDR driving within BT_PHC
Bit3-2	GDR driving within BT_PHB
Bit1-0	GDR driving within BT_PHA

RDBH(TEST): CPCK_ SEL

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	0	1	1	(DBH)
1st Parameter	W	1	0	0	0	0	0	0	CPCK_SEL		(03H)

CPCK_SEL	00:8Mhz, 01:1Mhz, 10:2Mhz, 11:4Mhz(default)

RDCH(TEST): CPCK SET enable

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	0	(DCH)
1st Parameter	W	1	0	0	0	0	0	0	CPCKDFEN	CPCKEN	(03H)

Bit0	CPCK enable 0:OFF 1:ON
Bit1	CPCKDFEN :CPCK PWH SET & CPCK PWL SET enable 1:follow default 0:follow RDDH & RDEH

RDDH(TEST): CPCK PWH SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	1	(DDH)
1st Parameter	W	1	CPCK PWH SET								(08H)

Adjust the sampling frequency of VDH/VDL/VDHR clamping.

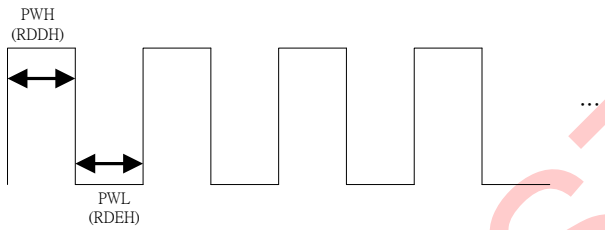
Bit7-0	CPCK PWH SET	Bit7-0	CPCK PWH SET
00H	0 ns	:	:
01H	125 ns	FCH	31500ns
02H	250 ns	FDH	31625ns
03H	375 ns	FEH	31750ns
04H	500 ns	FFH	31875ns

RDEH(TEST): CPCK PWL SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	1	0	(DEH)
1st Parameter	W	1	CPCK PWL SET								(08H)

Adjust the sampling frequency of VDH/VDL/VDHR clamping.

Bit7-0	
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns



RDFH(TEST): VD_Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	1	1	(DFH)
1st Parameter	W	1	0	0	VDHR_SEL		VDH_SEL		VDL_SEL		(3FH)

Bit5-4	VDHR driving	00:weak	11:strong
Bit3-2	VDH driving	00:weak	11:strong
Bit1-0	VDL driving	00:weak	11:strong

RA8H(TEST): VDHROS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	0	1	0	1	0	0	0	(A8H)
1st Parameter	W	1	0	0	1	1	1	1	1	VDHROS EN	(3FH)

Adjust the compensation driving of VDHR, which affects the waveform during VDHR switching.

Bit0	VDHR driving enable
0	VDHR driving OFF
1	VDHR driving ON(default)

RE8H(TEST): VDLOS_Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	0	0	0	(E8H)
1st Parameter	W	1	0	0	0	0	0	0	VDLOS_SEL		(01H)

Adjust the compensation driving of VDL, which affects the waveform during VDL switching.

Bit1-0	Adjusting VDL driving 00: strong 11:weak

RFDH(TEST): VDLOS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	0	1	(FDH)
1st Parameter	W	1	0	0	0	0	0	0	0	VDLOS EN	(01H)

Bit0	VDL compensation driving enable
0	VDL compensation driving OFF
1	VDL compensation driving ON(default)

RF9H(TEST): VGLOS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	0	0	1	(F9H)
1st Parameter	W	1	0	0	0	0	0	0	0	VGLOS EN	(01H)

Adjust the compensation driving of VGL

Bit0	VGL compensation driving enable
0	VGL compensation driving OFF
1	VGL compensation driving ON(default)

RCFH(TEST): VDLOS

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	0	1	1	1	1	(CFH)
1st Parameter	W	1	0	0	0	0	0	0	0	VDLOS	(01H)

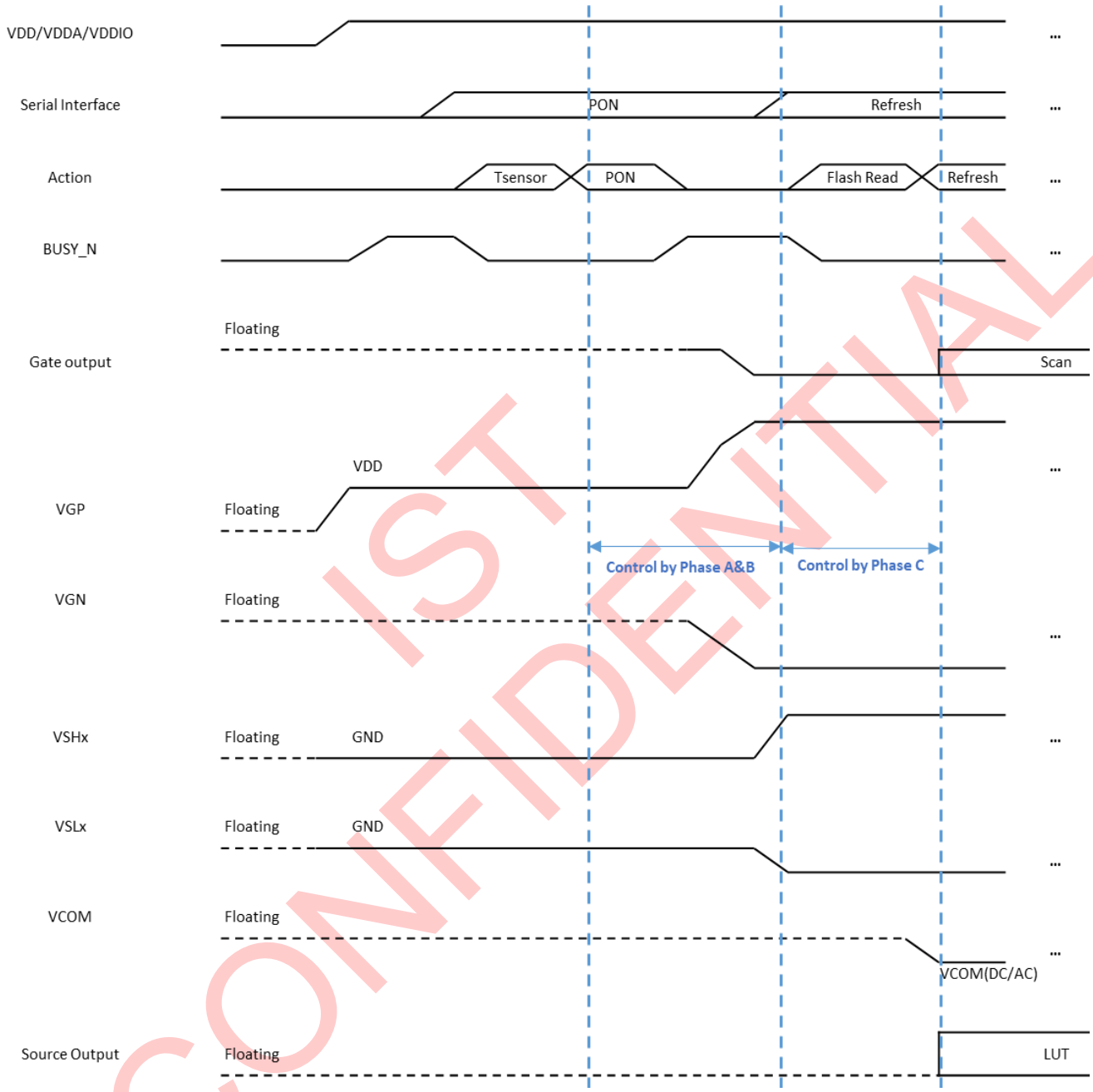
Adjust the O.S. of VDL

Bit0	VDL O.S
0	Small
1	Large (default)

FUNCTION DESCRIPTION

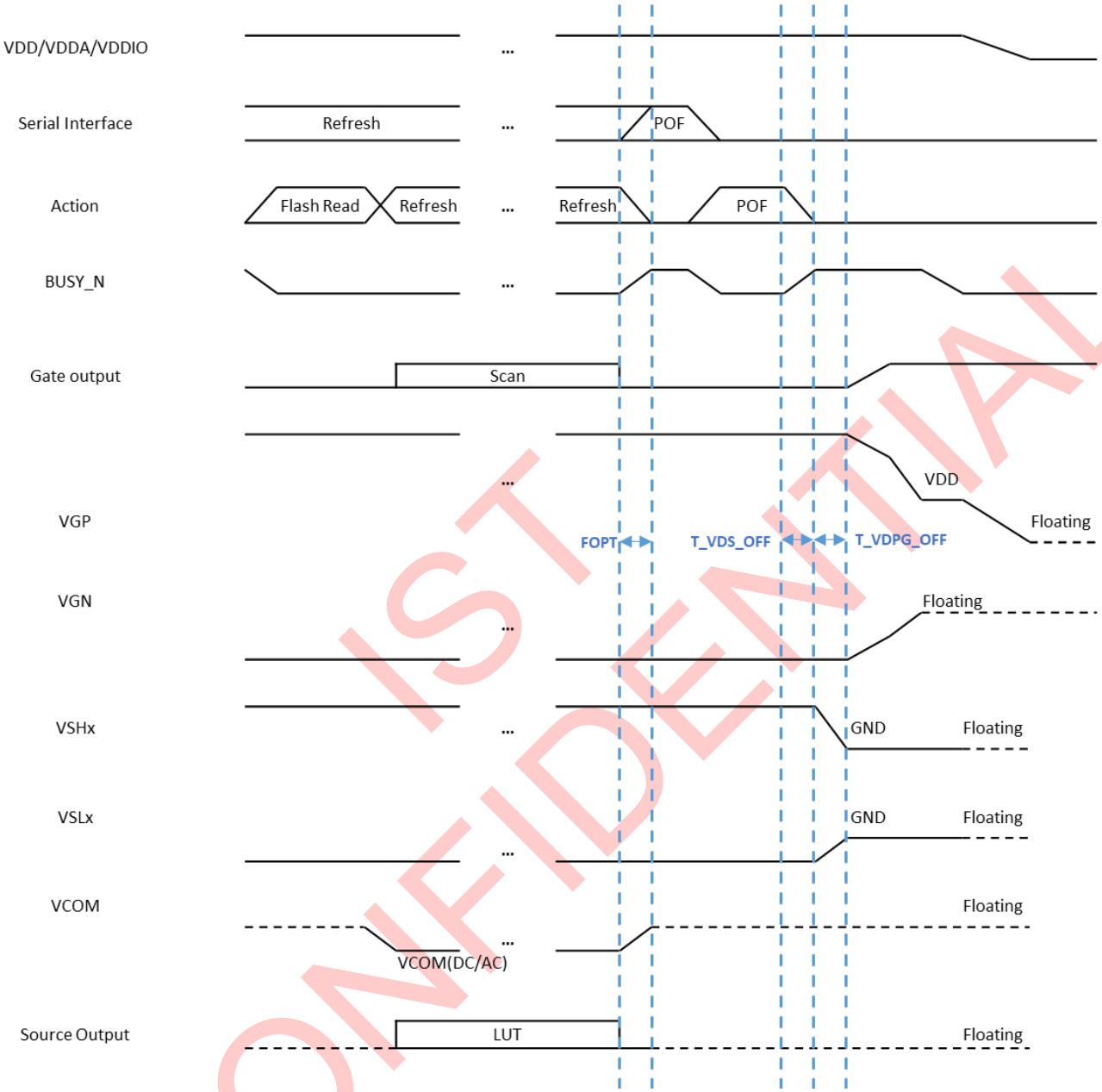
Power on sequence

Figure 1: Power on sequence

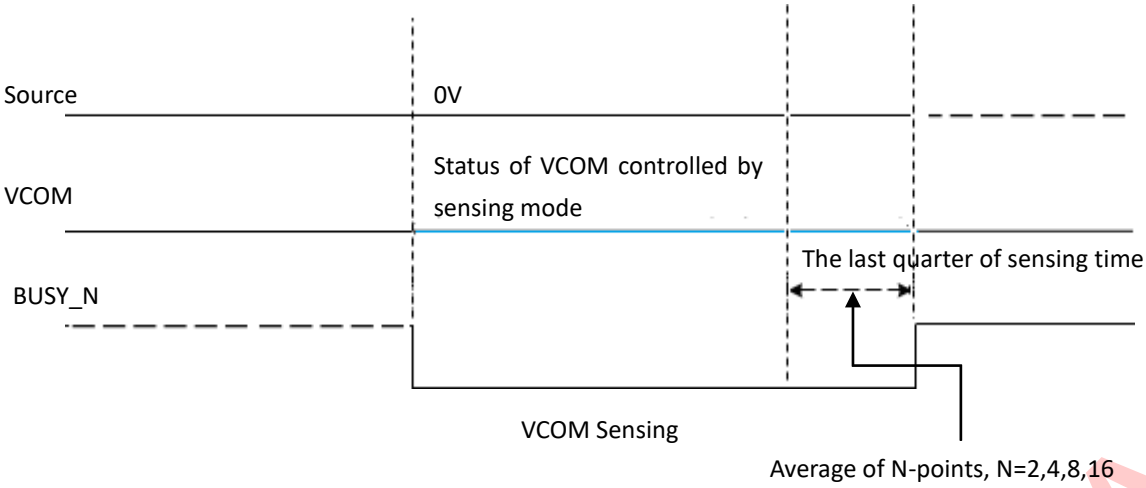


Power off sequence

Figure 2: Power off sequence



VCOM Sensing



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Supply voltage range	VDDIO/VDD1/2/3/5	- 0.3 to 5	V
	VDDLI/VDDLO	- 0.3 to 2	V
	VGH	-0.3 to 20	V
	VGL	0.3 to -20	V
	VDH	-0.3 to 18	V
	VDL	0.3 to -18	V
	VDHR	-0.3 to 18	V
	VCOMDC	0.3 to -8	V
	VCOMAC (VCOMH)	-0.3 to VGH	V
	VCOMAC (VCOML)	0.3 to VGL	V
Input voltage range	VIN	-0.3 to VDDIO+0.3	V
Operating temperature range	TOPR	-30 to +85	℃
Storage temperature range	TSTR	-55 to +125	℃

NOTES:

VDDIO/VDD1/2/3/5/VDDLI/VDDLOand VGH/VGL/VDH/VDL/VDHR/VCOMDC/VCOMAC are based on VSS1/2/3/4/5 = 0V.

If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.
It is desirable to use this LSI under electrical characteristic conditions during general operation.
Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

(Ta = -30 to 85℃)

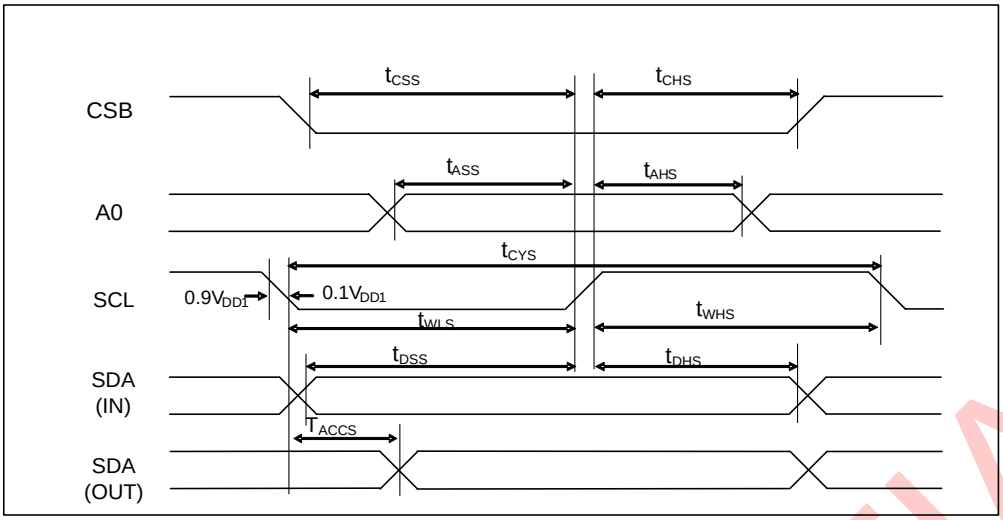
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		VDDIO		2.3	3.3	3.6	V
Supply Voltage		VDD1/2/3/5		2.3	3.3	3.6	V
Operation Voltage		VGH		10	-	20	V
Operation Voltage		VGL		-20	-	-10	V
Operation Voltage		VDH		3	-	15	V
Operation Voltage		VDHR		3	-	15	V
Operation Voltage		VDL		-15	-	-3	V
Operation Voltage		VCOMDC		-5	-	0	V
Operation Voltage		VCOMH		VDH+VCOMDC	-	VGH	V
Operation Voltage		VCOML		VGL	-	VDL+VCOMDC	V
Input Voltage	High	VIH		0.8*VDDIO	-	VDDIO	V
	Low	VIL		VSS1	-	0.2*VDDIO	
Output Voltage	High	VOH	IOUT = 1mA, VDDIO =2.4V	0.8*VDDIO	-	VDDIO	V
	Low	VOL	IOUT= -1mA, VDDIO =2.4V	VSS1	-	0.2*VDDIO	
Input Leakage Current		IIL	VIN= VDDIO or VSS1	-1.0	-	+1.0	μA
Driver Outputs ON Resistance		RON	Ta = 25℃, VDH=12V, VDL=-12V, VDHR=4V	-	-	10	kΩ
Oscillator Frequency (internal)		FOSC	Ta = 25℃	7.7	8.0	8.3	MHz
Refresh Current		IDD1 +IDD2 +IDD3 +IDD5 +IDDIO (Refer to the specified Application Circuit of the following page)	Ta=25℃ VDDIO=VDD1/2/3/5=3V VGH=20V,VGL=-20V VDH=15V,VDL=-15V (include External circuit , no load)		2.5		mA
Deep Sleep Current		IVDD	Pattern no update, OSC off, VDD1/2/3/5=3.0V, Ta=25 ℃	-	1		uA(*1)

Note：

(*1) In Deep sleep mode, the SDA will be in Output state and to be pulled High internall to VDDIO. It’s recommended MCU settingSDA as Hi-Z to avoid leakage.

AC CHARACTERISTICS

Serial Interface Characteristics



SPI Write(VDDIO=2.3 to 3.6V, Ta = -30 to +85℃)

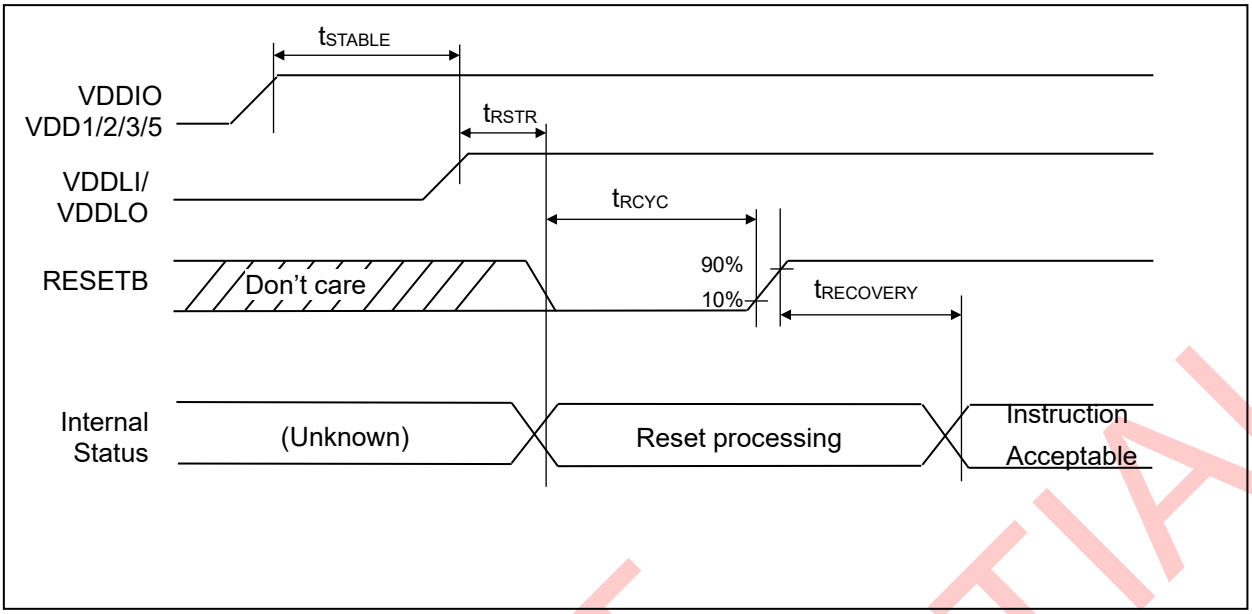
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	SCL	tcys	50	-	-	ns	
SCL high pulse width		twhs	25	-	-		
SCL low pulse width		twls	25	-	-		
Address setup time	A0	tass	5	-	-	ns	
Address hold time		tahs	5	-	-		
Data setup time	SDA	tdss	30	-	-	ns	
Data hold time		tdhs	30	-	-		
CSB setup time	CSB	tcss	60	-	-	ns	
CSB hold time		tchs	65	-	-		

SPI Read (VDDIO=2.3 to 3.6V, Ta = -30 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	SCL	tcys	600	-	-	ns	
SCL high pulse width		twhs	150	-	-		
SCL low pulse width		twls	400	-	-		
Address setup time	A0	tass	90	-	-	ns	
Address hold time		tahs	90	-	-		
Read access time	SDA	taccS	-	-	200	ns	
CSB setup time	CSB	tcss	400	-	-	ns	
CSB hold time		tchs	150	-	-		

Note: All signal Rising time and falling Time <15ns

Reset Input Timing



(VDDIO=2.3 to 3.6V, VDD1/2/3/5 = 2.3 to 3.6V, Ta = -30 to +85℃)

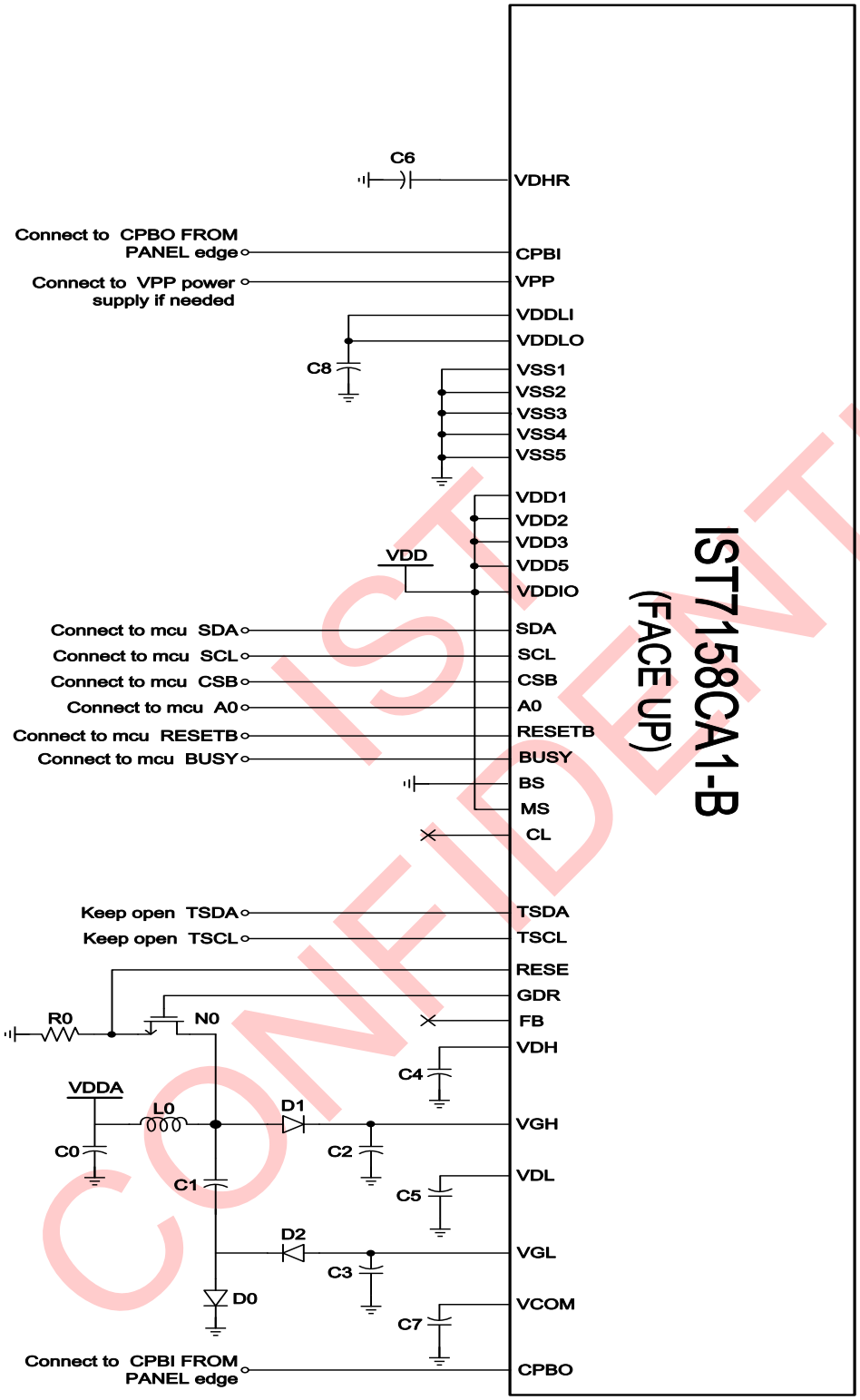
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
VDDIO/VDD1/2/3/5 stable time	VDDIO VDD1/2/3/5	tSTABLE	10	-	-	ms	With external Cap (*1)
Reset start time	RESETB	tRSTR	0	-	-	us	
Reset cycle time	RESETB	tRCYC	1	-	-	ms	
Reset recovery time	RESETB	tRECOVERY	1	-	-	ms	(*2)

NOTE

*1. tSTABLE depending on different capacitance of Capconnect to VDDLI/VDDLO(external stabilizing capacitor), and It should be re-adjusted for different capacitance of the Cap connect to VDDLI/VDDLO.

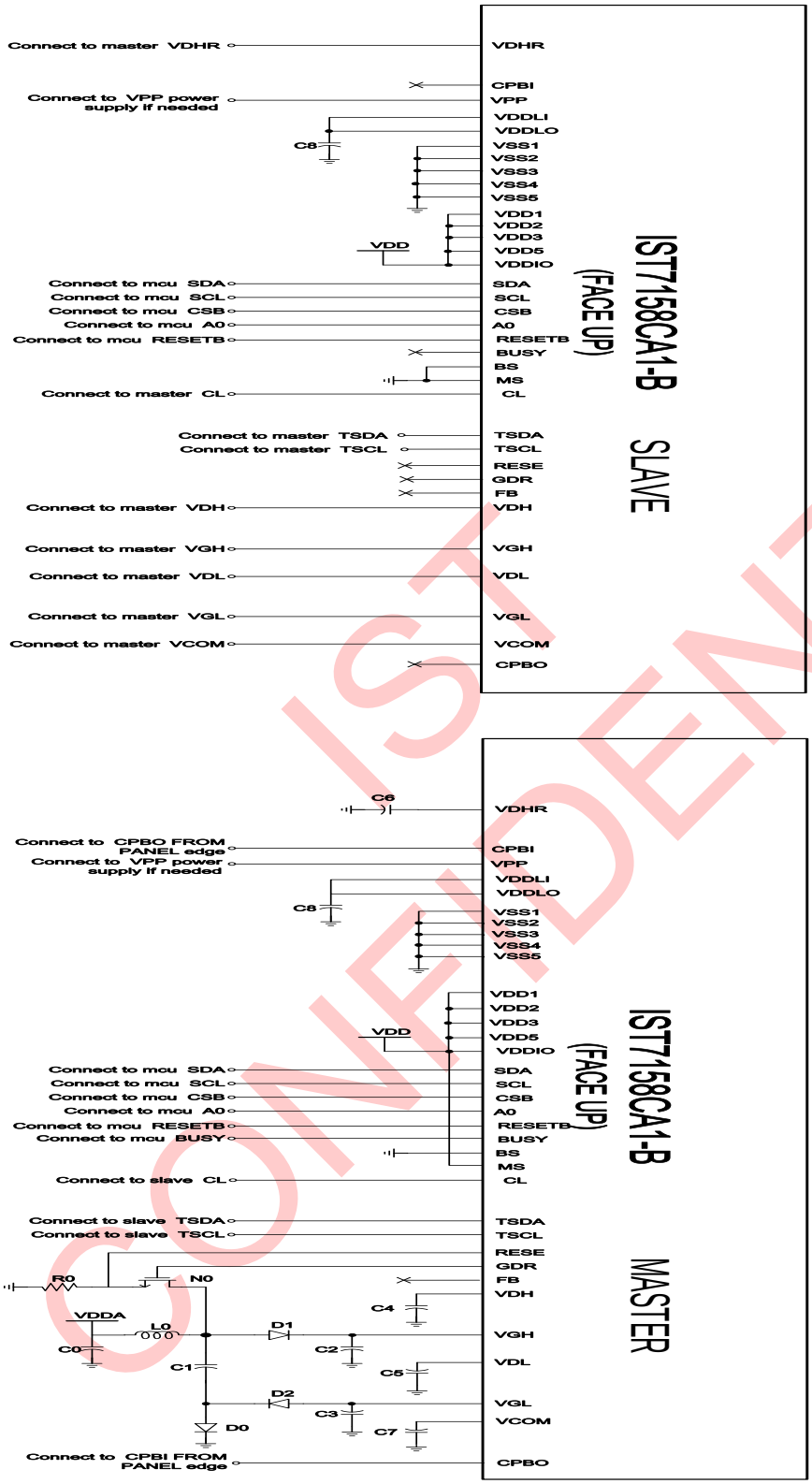
*2. After reset 1ms, it must check that the BSUY_N signal is high before the first instruction can be executed.

Application Circuit (Single chip)



Component	Item	Recommendation
Inductor	L0	10uH/47uH
Resistor	R0	0.47Ω/2.2Ω，0603/0805，1% variation
Capacitor	C0/ C1	1uF/4.7uF/25V，0603/0805，X5R/X7R
	C2/C3/C4	1uF/25V，0603/0805，X5R/X7R
	C5	1uF/25V，0805，X5R/X7R
	C6/ C7/C8	1uF/25V，0603/0805，X5R/X7R
Diode	D0/D1/D2	IF>= 2A
N-MOSFET	N0	ID>= 2A

Application Circuit (Master and Slave)



Note:

1. Slave initial code remove Power on command

2. Make sure Master and Slave use the same Lut-table

Component	Item	Recommendation
Inductor	L0	10uH/47uH
Resistor	R0	0.47Ω/2.2Ω，0603/0805，1% variation
Capacitor	C0/ C1	1uF/4.7uF/25V，0603/0805，X5R/X7R
	C2/C3/C4	1uF/25V，0603/0805，X5R/X7R
	C5	1uF/25V，0805，X5R/X7R
	C6/ C7/C8	1uF/25V，0603/0805，X5R/X7R
Diode	D0/D1/D2	IF>= 2A
N-MOSFET	N0	ID>= 2A

CAUTIONS:

1. This Specification will be subjected to modify without notice.
2. Precautions on Light:

Characteristics of semiconductor devices can be changed when exposed to light as described in the operational principles of solar batteries. Exposing this IC to light, therefore, can potentially lead to its malfunctioning.

2.1 Care must be exercised in designing the operation system and mounting the IC so that it may not be exposed light during operation.

2.2 Care must be exercised in designing the inspection process and handling the IC so that it may not be exposed to light during the process.

2.3 The IC must be shielded from light in the front, back and side faces.

3. ESD control and prevention:

3.1 Humidity Control: 30~70% relative humidity is recommended.

3.2 To reduce the risk of ESD, all equipment at the wok surface should be properly grounded and all sources of static fields removed.(Example: Station ionizers).

3.3 Grounding all personnel who come in contact with parts will eliminate a possible source of ESD. (Example: Wrist straps remove charge from the body and constitute a central part of ESD control).

4. Storage Conditions:

Before open package	After open package
Temp.=25±5℃ Humidity:50~70% Less than 1 Years	Temp.=25±5℃ Humidity:50~70% Less than 3 Months