5.79 inch
E-paper Display Series

GooDisplay®

GDEY0579F52

Dalian Good Display Co., Ltd.

Product Specifications

Customer	Standard
Description	ePaper Display
Model Name	GDY0579F52
Date	2025/06/26
Revision	1.0

	Design Engineering		
	Approval	Check	Design
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Content

1. Overview

GDEY0579F52 is a reflective electrophoretic technology display module on anactive matrix TFT substrate. The panel is capable of displaying black, white, yellow and redimages depending on the associated lookup table used. The circuitry on the panel includes anintegrated gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memoryto store the framebuffer and lookup tables, and additional circuitry to control VCOM and BORDER settings.

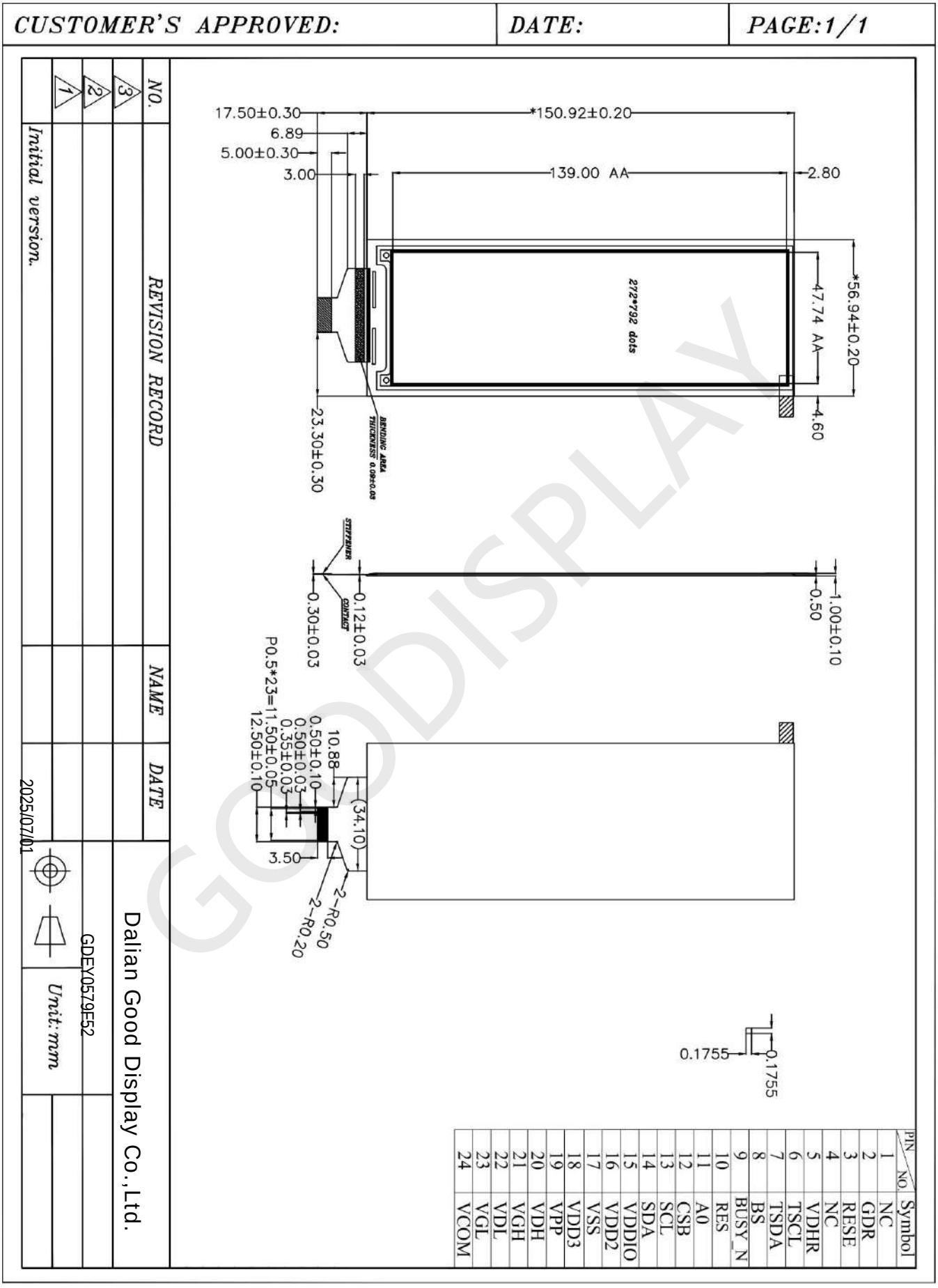
2. Features

- Highlight Red and Yellow color
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I^2C signal master interface to read external
- Temperature sensorAvailable in COG package

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	5.79	Inch	
Display Resolution	272(H)×792(V)	Pixel	Dpi:144
Active Area	47.74×139.00	mm	
Pixel Pitch	0.1755×0.1755	mm	
Pixel Configuration	Rectangle		
Outline Dimension	56.94 (H)×150.92(V) ×1.0(D)	mm	
Weight	15.7±0.5	g	

4. Mechanical Drawing of EPD module



5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Not Connected	
2	GDR	O	N-MOS gate control, for booster circuit output	
3	RESE	O	Current sense input for control loop.	
4	NC		Not Connected	
5	VDHR	I/O	Positive source driver voltage for Red	
6	TSCL	O	I2C clock for external temperature sensor	
7	TSDA	I/O	I2C datafor external temperature sensor	
8	BS	I	Bus Selection.	
9	BUSY_N	O	Driver busy flag.	
10	RES	I	Global reset pin. Low: reset.	
11	A0	I	When SPI3 is select A0=H mean writing the command index to IST7158CA1 A0=L mean writing command data or display data to IST7158CA1	
12	CSB	I	Serial communication chip select.	
13	SCL	I	Serial communication clock input.	
14	SDA	I/O	Serial communication data input/output	
15	VDDIO	P	IO power	
16	VDD2	P	Analog power	
17	VSS	P	Ground	
18	VDD3	P	Analog power	
19	VPP	P	OTP power	
20	VDH	I/O	Positive source driver Voltage	
21	VGH	I/O	Positive gate voltage	
22	VDL	I/O	Negative source driver voltage	
23	VGL	I/O	Negative Gate voltage.	
24	VCOM	O	VCOM output	

Note: I: Input, O: Output, P: Power, I/O: Input / Output. P: Power

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Supply voltage range	VDDIO/VDD2/VDD3	- 0.3 to 5	V
	VDDLI/VDDLO	- 0.3 to 2	V
	VGP	-0.3 to 20	V
	VGN	0.3 to -20	V
	VSH1	-0.3 to 18	V
	VSL	0.3 to -18	V
	VSH2	-0.3 to 12	V
	VCOMDC	0.3 to -8	V
	VCOMAC (VCOMH)	-0.3 to VGP	V
	VCOMAC (VCOML)	0.3 to VGN	V
Input voltage range	VIN	-0.3 to VDDIO+0.3	V
Operating Temp range	TOPR	0 to +40	°C
Storage Temp range	TSTG	-25 to +70	°C
Optimal Storage Temp	TSTGo	23±2	°C
Optimal Storage Humidity	HSTGo	55±10	%RH

NOTES:

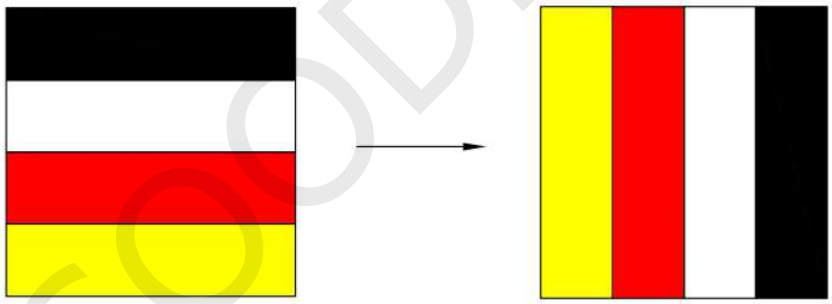
VDDIO/VDD2/VDD3/VDDLI/VDDLO and VGP/VGN/VSH1/VSL/VSH2/VCOMDC/ VCOMACare based on VSS1/VSS2/VSS3/VSS4 = 0V.

If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

6.2 Panel DC Characteristics

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Supply Voltage	VDDIO	-	VDDIO	2.3	3.3	3.6	V
Supply Voltage	VDD2/3		VDD2/3	2.3	3.3	3.6	V
High level input voltage	V_{IH}	-	-	0.8VDDIO	-	VDDIO	V
Low level input voltage	V_{IL}	-	-	VSS1	-	0.2VDDIO	V
High level output voltage	V_{OH}	IOUT=1mA, VDDIO=2.4V	-	0.8VDDIO	-	VDDIO	V
Low level output voltage	V_{OL}	IOUT= -1mA, VDDIO=2.4V	-	VSS1	-	0.2VDDIO	V
Typical power	P_{TYP}	V_{DD} =3.3V	-	-	41.4	-	mW
Deep sleep mode	P_{STPY}	V_{DD} =3.3V	-	-	0.003	-	mW
Typical operating current	Iopr_V_{DD}	V_{DD} =3.3V	-	-	13.8	-	mA
Full / Fast update time	-	25 ℃	-	-	20/12	-	sec
Deep Sleep Current	Ist_V_{DD}		-	-	1	5	uA
Stand-by Current	Ist_V_{DD}		-	-	30	40	uA

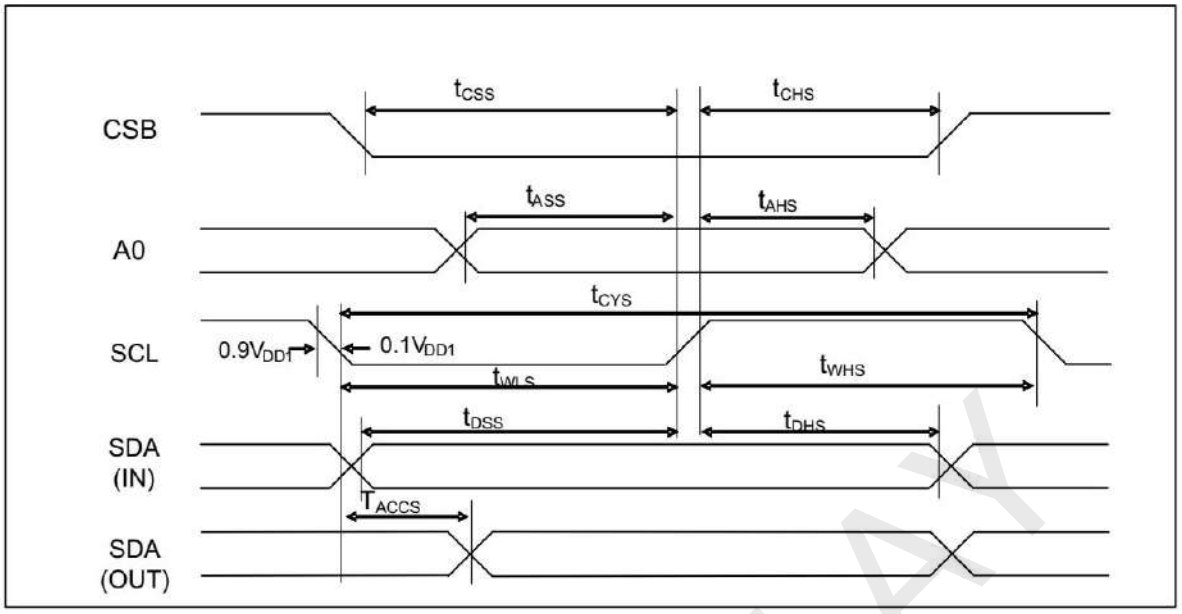
Notes: 1. The typical power is measured with following transition from horizontal 4 scale pattern tovertical 4 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveformprovided by NEWFACE.
4. Electrical measurement：Multimeter

6.3 AC Characteristics

Serial Interface Characteristics



SPI Write(VDDIO=2.3 to 3.6V, Ta = -30 to +85℃)

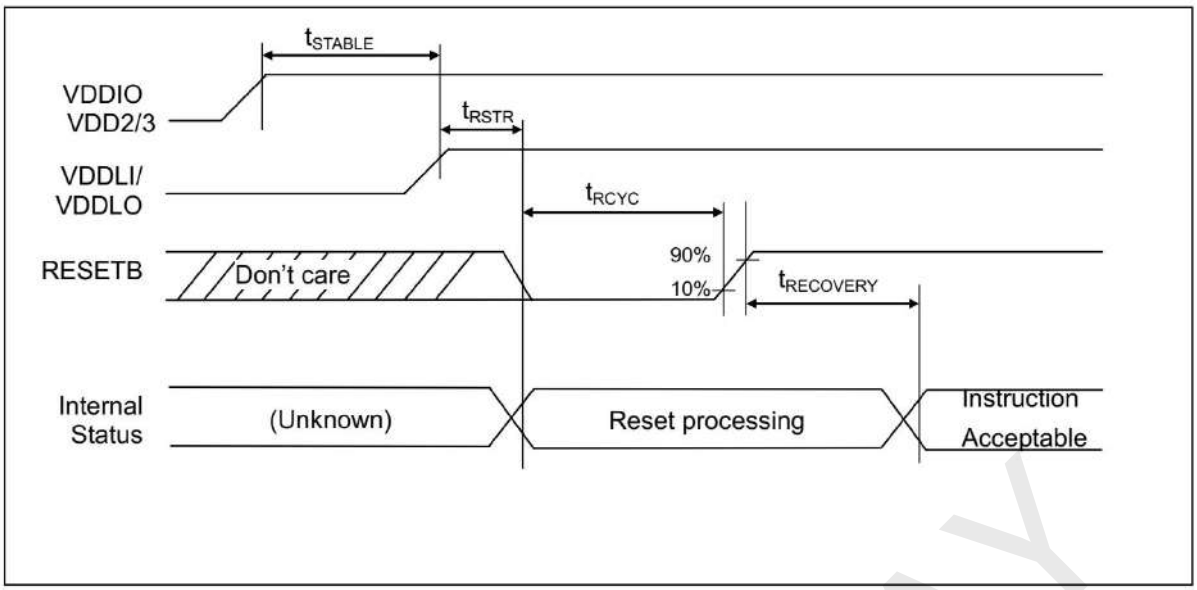
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	SCL	tcys	50	-	-	ns	
SCL high pulse width		twhs	25	-	-		
SCL low pulse width		twls	25	-	-		
Address setup time	A0	tass	5	-	-	ns	
Address hold time		tahs	5	-	-		
Data setup time	SDA	tdss	30	-	-	ns	
Data hold time		tdhs	30	-	-		
CSB setup time	CSB	tcss	60	-	-	ns	
CSB hold time		tchs	65	-	-		

SPI Read (VDDIO=2.3 to 3.6V, Ta = -30 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	SCL	tcys	600	-	-	ns	
SCL high pulse width		twhs	150	-	-		
SCL low pulse width		twls	400	-	-		
Address setup time	A0	tass	90	-	-	ns	
Address hold time		tahs	90	-	-		
Read access time	SDA	taccS	-	-	200	ns	
CSB setup time	CSB	tcss	400	-	-	ns	
CSB hold time		tchs	150	-	-		

Note: All signal Rising time and falling Time <15ns

Reset Input Timing



(VDDIO=2.3 to 3.6V, VDD2/3 = 2.3 to 3.6V, Ta = -30 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
VDDIO/VDD2/VDD3 stable time	VDDIO/VDD2 /VDD3	tSTABLE	10	-	-	ms	With external Cap (*1)
Reset start time	RESETB	tRSTR	0	-	-	us	
Reset cycle time	RESETB	tRCYC	1	-	-	ms	
Reset recovery time	RESETB	tRECOVERY	1	-	-	ms	(*2)

NOTE

*1. tSTABLE depending on different capacitance of Capconnect to VDDLI/VDDLO(external stabilizing capacitor), and It should be re-adjusted for different capacitance of the Cap connect to VDDLI/VDDLO.

*2. The first instruction should only be issued after the internal reset processing has been completed.

7. Command Table

R00H(PSR): Panel setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PSR	W	0	0	0	0	0	0	0	0	0	(00H)
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	1	(0FH)
2nd Parameter	W	1	LUT_EN	0	FOPT	VCMZ	1	TIEG	NORG	VC_LUTZ	(09H)

1st Parameter:

Bit7-6	Resolution setting
00b	Display resolution is 400x300 (default)
01b	Display resolution is 300x300
10b	Display resolution is 256x256
11b	Display resolution is 128x128

Bit5	Power switch operation mode
0	Power switching time in the period of frame scanning.(default).
1	Power switching time in the external period before frame scanning.

Bit3	UD function(*1)
0	Scandown; First line=Gn,Gn-1, ... G2, Last line=G1
1	Scanup; First line=G1,G2, ... ,Gn-1, Last line=Gn.(default)

Bit2	SHL function(*2)
0	Shift left; First data=Sn,Sn-1, ... ,S2, Last data=S1.
1	Shift right; First data=S1,S2, ... ,Sn-1, Last data=Sn.(default)

Bit1	SHD_N function(*3)
0	Booster OFF, register data are kept,and Source/Border/VCOM are kept 0V or floating
1	Booster ON.(default)

2nd Parameter:

Bit0	VC_LUTZ function
0	NO effect.
1	After refreshing display,the output of VCOM is set to floating automatically(default)

Bit1	NORG function
0	NO effect.(default)
1	After refreshing display,VCOM is tied to GND before power off

Bit2	TIEG function
0	NO effect.(default)
1	After power off booster,VGL will be tied to GND.

Bit4	VCMZ function
0	NO effect.(default)
1	VCOM is always floating.

Bit5	FOPT function
0	Scan 1 frame after waveform finished (Default)
1	No Scan after waveform finished and switch the source channel output to HiZ

Bit7	LUT_EN
0	LUT from OTP(default)
1	LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.

FOPT: Power off floating.

Notes:

1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Inactive source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R01H(PWR): Power Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWR	W	0	0	0	0	0	0	0	0	1	(01H)
1st Parameter	W	1	-	-	-	-	V_MODE	VSC_EN	VS_EN	VG_EN	(07H)
2nd Parameter	W	1	-	-	-	-	-	-	VG[1]	VG[0]	(00H)
3rd Parameter	W	1	-	VDHR [6]	VDHR [5]	VDHR [4]	VDHR [3]	VDHR [2]	VDHR [1]	VDHR [0]	(00H)
4th Parameter	W	1	-	VDH [6]	VDH [5]	VDH [4]	VDH [3]	VDH [2]	VDH [1]	VDH [0]	(00H)
5th Parameter	W	1		VDL[6]	VDL [5]	VDL [4]	VDL [3]	VDL [2]	VDL [1]	VDL [0]	(00H)
6th Parameter	W	1		VDHR1 [6]	VDHR1 [5]	VDHR1 [4]	VDHR1 [3]	VDHR1 [2]	VDHR1 [1]	VDHR1 [0]	(00H)

Power mode switch mapping:

Mode 0 : 0V & +15V & -15V & VDHR (+3V~+15V)

Mode 1 : 0V & VDH (+3V~+15V) & VDL (-3V~-15V) & VDHR1 (+3V~+15V)

1st Parameter:

Bit3	Initial source power mode.
0	Mode0. (default)
1	Mode1.

Bit2	Source LV power selection.
0	External source LV power from VDHR pins.
1	Internal DC/DC function for generate VDHR.

Bit1	Source power selection.
0	External source power from VDH/VDL pins.
1	Internal DC/DC function for generate VDH/VDL.

Bit0	Gate power selection.
0	External gate power from VGH/VGL pins.
1	Internal DCDC function for generate VGH/VGL.

2nd Parameter:

Bit1-0	VGH & VGL Voltage Level.
00	VGH=20v, VGL=-20v(default)
01	VGH=17v, VGL=-17v
10	VGH=15v, VGL=-15v
11	VGH=10v, VGL=-10v

3rd & 4th Parameter: Internal VDHR/VDH power selection (Default value: 0000000b)

5th & 6th Parameter: Internal VDL/VDHR1 power selection (Default value: 0000000b)

Bit6-0	Internal VDH selection.	Internal VDL selection.	Bit6-0	Internal VDH selection.	Internal VDL selection.
0000000	3V	-3V	0110010	8.0V	-8.0V
0000001	3.1V	-3.1V	...	...	...
0000010	3.2V	-3.2V	0111100	9.0V	-9.0V
0000011	3.3V	-3.3V	...	...	...
0000100	3.4V	-3.4V	1000110	10.0V	-10.0V
0000101	3.5V	-3.5V	...	...	...
0000110	3.6V	-3.6V	1010000	11.0V	-11.0V
0000111	3.7V	-3.7V	...	...	...
0001000	3.8V	-3.8V	1011010	12.0V	-12.0V
0001001	3.9V	-3.9V	...	...	...
0001010	4.0V	-4.0V	1100100	13.0V	-13.0V
0001011	4.1V	-4.1V	...	...	...
0001100	4.2V	-4.2V	1101110	14.0V	-14.0V
0001101	4.3V	-4.3V	...	...	...
0001110	4.4V	-4.4V	1111000	15.0V	-15.0V
0001111	4.5V	-4.5V			
0010000	4.6V	-4.6V			
...	...	...			
0010100	5.0V	-5.0V			
...	...	...			
0011110	6.0V	-6.0V			
...	...	...			
0101000	7.0V	-7.0V			
...	...	...			

Notes:

1. If gate voltage is set to +/-17v, +/-15v, +/-10v, IC will auto correct source voltage as follows:
2. VGH-VDH/VDH/VDHR1 ≧ 2v
3. VGL-VDL ≧ -2v

R02H(POF): Power OFF Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
POF	W	0	0	0	0	0	0	0	1	0	(02H)
1st Parameter	W	1	-	-	-	-	-	-	-	EDSE	(00H)

After power off command, driver will power off base on power off sequence. After power off command, BUSY_N signal will become "0".

Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register will keep until VDD become off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R03H(POFS): Power on/off Sequence Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PFS	W	0	0	0	0	0	0	0	1	1	(03H)
1st Parameter	W	1	-	-	T_VDPG_OFF		-	-	T_VDS_OFF		(00H)

1st Parameter:

Bit1-0	Power off sequence of VDH and VDL
00b	20ms(default)
01b	40ms
10b	60ms
11b	80ms

Bit5-4	Power off sequence of VGH and VGL
00b	20ms(default)
01b	40ms
10b	60ms
11b	80ms

R04H(PON):Power ON Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PON	W	0	0	0	0	0	0	1	0	0	(04H)

After power on command, the driver will power ON base on Power ON sequence.

After power on command and all power sequence are ready (based on PWR command), then BUSY_N signal will become "1".

This command only active when BUSY_N="1".

R06H(BTST): Booster Soft Command Reglster

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LUT0	W	0	0	0	0	0	0	1	1	0	(06H)
1st Parameter	W	1	BT_PHA1	BT_PHA0	0	0	0	0	0	0	(00H)
2st Parameter	W	1	BT_PHB1	BT_PHB0	0	0	0	0	0	0	(00H)
3st Parameter	W	1	BT_PHC1	BT_PHC0	0	0	0	0	0	0	(00H)

Control of Power On time.

D7-D6	BT_PHA/B/C perild
00	10ms (default)
01	20ms
10	30ms
11	40ms

R07H(DSLP): Deep Sleep Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSLP	W	0	0	0	0	0	0	1	1	1	(07H)
1st Parameter	W	1	1	0	1	0	0	1	0	1	(A5H)

After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excited if check code = 0xA5.

R10H(DTM): Data Start Transmission Register

`	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DTM	W	0	0	0	0	1	0	0	0	0	(10H)
2-bit mode											
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		(00H)
⋮	W	1	⋮		⋮		⋮		⋮		(00H)
Nth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		(00H)

NOTE:"-" Don't care, can be set to VDD or GND level. "X": Dummy data, it would not be stored in frame buffer.

This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data for panel.

Pixel[1~n][1:0](2-bit mode):

`	Source Driver Output			
ImageData	DDX=1(Default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00	Gray0	ogray00	Gray3	ogray03
01	Gray1	ogray01	Gray2	ogray02
10	Gray2	ogray02	Gray1	ogray01
11	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1, Pixel[1:0]=01 -> Gray level select = Gray1, follow LUT data output from IP output port "ogray01".

When DDX=0, Pixel[1:0] = 11 -> Gray level select = Gray 0, follow LUT data output from IP output port "ogray00".

R11H(DSP): DataStop Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSP	W	0	0	0	0	1	0	0	0	1	(11H)
1st Parameter	R	1	data_flag	-	-	-	-	-	-	-	(00H)

To stop data transmission,this command must be issued to check the data_flag.

1st Parameter:

Bit7	Data flag of receiving user data.
0	Driver didn't receive all the data.
1	Driver has already received all the one frame data.

After "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.

This command only active when BUSY_N = "1".

R12H(DRF): Display Refresh Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DRF	W	0	0	0	0	1	0	0	1	0	(12H)
1st Parameter	W	1	-	-	-	-	-	-	-	AC/DCVCOM	(00H)

While user sent this command,driver will refresh display(data/VCOM) base on SRAM data and LUT.

AC/DCVCOM: AC,DC VCOM select.

0: ACVCOM,VCOM will follow LUTC when updating image. (default)

1: DCVCOM,VCOM will always be VCOMDC when updating image

After display refresh command, BUSY_N signal will become "0"

This command only active when BUSY_N = "1".

R17H(AUTO): Auto Sequence Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Auto Sequence	W	0	0	0	0	1	0	1	1	1	(17H)
	W	1	1	0	1	0	0	1	0	1	(A5H)

The command can enable the internal sequence to execute several commands continuously.

The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO(0x17)+Code(0xA5)=(PON → DRF → POF)

AUTO(0x17)+Code(0xA7)=(PON → DRF→ POF → DSLP)

R20H(LUT0): LUT0 Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LUT0	W	0	0	0	1	0	0	0	0	0	(20H)
1st Parameter	W	1	Data 0								(00H)
.....		1	.....								(00H)
535th Parameter	W	1	Data 534								(00H)

Write LUT0 register from MCU interface

R30H(PLL): PLL Control Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PLL	W	0	0	0	1	1	0	0	0	0	(30H)
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	(02H)

The command controls the PLL clock frequency.The PLL structure must support the following frame rates:

Bit3	Dynamic frame rate (EInk use only)
0	Disable(default)
1	Enable

FR[2:0]	Framerate
000	12.5 Hz
001	25 Hz
010	50 Hz (default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

R40H(TSC): Temperature Sensor Command Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	0	0	0	0	0	0	(40H)
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	(00H)

This command indicates the temperature value.
If R41H(TSE) bit7 set to 0, this command reads temperature sensor value.

BUSY_N become low after TSC command. When BUSY_N become high, Parameter can be read.
This command only active when BUSY_N="1"

Temperature boundary: -25C~60C

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
...	...
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
...	...
0011_1011	59
0011_1100	60

R41H(TSE): Temperature Sensor Enable Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSE	W	0	0	1	0	0	0	0	0	1	(41H)
1st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	(00H)

This command indicates the driver IC temperature sensor enable and calibration function.

1st Parameter:

Bit7	Internal temperature sensor enable
0	Enable internal temperature sensor. (default)
1	Disable internal temperature sensor, using external temperature sensor.

Bit3-0	Temperature level	Bit3-0	Temperature level
0000	+0℃ (Default)	1000	-4℃
0001	+0.5℃	1001	-3.5℃
...	...	...	...
0111	+3.5℃	1111	-0.5℃

Bit[3:0]: Reserve one temperature offset TO[3:0] for calibration

1. TO[3]: mean "+" or "-" while 0 is "+"; 1 is "-"

2. TO[2:0]: mean temperature offset value

R44H(GPI Sensing): GPIO Input Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Check Panel Glass	W	0	0	1	0	0	0	1	0	0	(44H)
	W	1	-	-	-	-	-	-	-	GPIS	(00H)

This command will indicate status of GPI

GPIS : 0 detected low logic on GPIO

1 detected high logic on GPIO

R50H(CDI): VCOM and DATA Interval Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CDI	W	0	0	1	0	1	0	0	0	0	(50H)
1st Parameter	W	1	VBD[2]	VBD[1]	VBD[0]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	(97H)

This command can set 2 kinds of parameters,1.VCOM to data output interval(CDI) 2.Border pin output.

VBD[2:0]: Border data selection (from LUT output by IP port border_w[1:0]).

This register will make border pin output being mapped to a certain grayscale.

DDX[0]	VBD[2:0]	Gray level select	IP setting for Border LUT select
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (Default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating(Default)	N/A

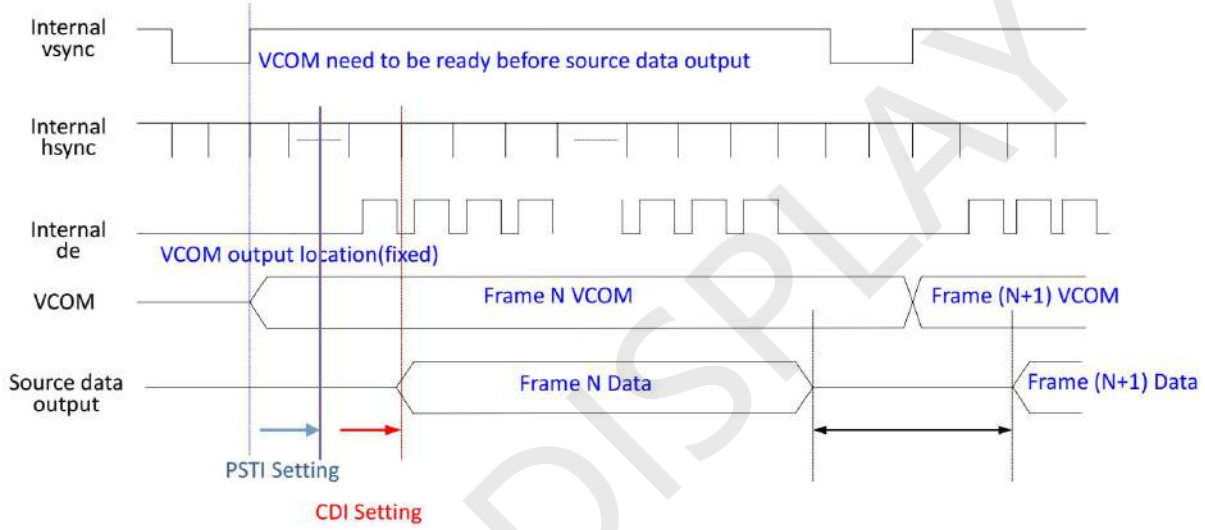
Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V, without VCOM offset,the real output on Border pin shall be 15V+VCOMDC.

Border output will follow FOPT definition being defined in R00h

This command indicates the interval of Vcom and data output.When setting the vertical backporch, the total blanking will be kept as a default value (count by HSYNC)

Bit3	Bit2	Bit1	Bit0	VCOM and data interval
0	0	0	0	17 hsync
0	0	0	1	16 hsync
0	0	1	0	15 hsync
0	0	1	1	14 hsync
0	1	0	0	13 hsync
0	1	0	1	12 hsync
0	1	1	0	11 hsync
0	1	1	1	10 hsync (Default)
1	0	0	0	9 hsync.
1	0	0	1	8 hsync
1	0	1	0	7 hsync
1	0	1	1	6 hsync
1	1	0	0	5 hsync
1	1	0	1	4 hsync
1	1	1	0	3 hsync
1	1	1	1	2 hsync



R51H(LPD): Lower Power Detection Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LPD	W	0	0	1	0	1	0	0	0	1	(51H)
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	(01H)

This command indicates the input power condition. Host can read this data to understand the battery condition.

When LPD="1",system input power is normal.

When LPD="0",Low power input (VDD<2.5V,selected by LVD_SEL[1:0] in command LVSEL)

Bit0	LPD
0	Lowpowerinput.
1	Normalstatus.(Default)

This command only active when BUSY_N="1".

R60H (TCON): TCON setting Register

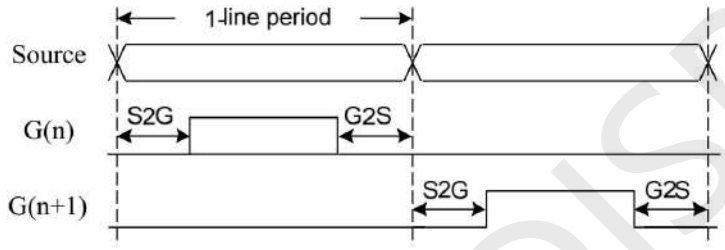
Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	1	0	0	0	0	0	(60H)
1st Parameter	W	1	-	-	S2G[5]	S2G[4]	S2G[3]	S2G[2]	S2G[1]	S2G[0]	(02H)
2nd Parameter	W	1	-	-	G2S[5]	G2S[4]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	(02H)

The command define as Non-overlap period of gate and source and as below:

S2G[5:0] or G2S[5:0]	Period
0	1unit
1	2unit
2	3unit(Default)
3	4unit
4	5unit
5	6unit
6	7unit
7	8unit
8	9unit
9	10unit
10	12unit
11	14unit
12	16unit
13	18unit
....	...
63	118unit

1 unit = 500ns

Gon_T= 1 line period – S2G –G2S, minimum Gon_T = 2 units. If(1line period – S2G –G2S) <2 units , Gon_T = 2 units



R61H(TRES): Resolution Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TRES	W	0	0	1	1	0	0	0	0	1	(61H)
1st Parameter	W	1	0	0	0	0	0	0	0	HRES(8)	(00H)
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	(00H)
3rd Parameter	W	1	0	0	0	0	0	0	0	VRES(8)	(00H)
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	(00H)

Note: HRES ≦ Horizontal line of PSR, VRES ≦ Vertical line of PSR.

No matter what value being set in D1 and D0 of 1st parameter(HRES[1] and HRES[0]), the register shall be kept as 0

When using register:

Horizontal display resolution = HRES

Vertical display resolution = VRES

Channel disable calculation:

GD: First G active=G0; LAST active GD = first active+VRES[8:0]-1

SD: First active channel:=S0; LAST activeSD = first active+HRES[8:2]*4-1

R65H(GSST): GATE/SOURCE START SETTING

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GSST	W	0	0	1	1	0	0	1	0	1	(65H)
1st Parameter	W	1	0	0	0	0	0	0	0	HST (8)	(00H)
2nd Parameter	W	1	HST (7)	HST (6)	HST (5)	HST (4)	HST (3)	HST (2)	0	0	(00H)
3rd Parameter	W	1	0	0	0	0	0	0	0	VST (8)	(00H)
4th Parameter	W	1	VST (7)	VST (6)	VST (5)	VST (4)	VST (3)	VST (2)	VST (1)	VST (0)	(00H)

This command defines resolution start gate/source position.

HST[8:2]: Horizontal Display Start Position (Source)

VST[8:0]:Vertical Display Start Position (Gate)

R70H(REV): Chip Revision Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
REV	W	0	0	1	1	1	0	0	0	0	(70H)
1st Parameter	R	1	REV0[7]	REV0[6]	REV0[5]	REV0[4]	REV0[3]	REV0[2]	REV0[1]	REV0[0]	(05H)
2nd Parameter	R	1	REV1[7]	REV1[6]	REV1[5]	REV1[4]	REV1[3]	REV1[2]	REV1[1]	REV1[0]	(04H)
3rd Parameter	R	1	REV2[7]	REV2[6]	REV2[5]	REV2[4]	REV2[3]	REV2[2]	REV2[1]	REV2[0]	(01H)

1nd Parameter:

Bit7-0	REV0
-	Elnk internal number

2nd Parameter:

Bit7-0	REV1
-	Elnk internal number

3rd Parameter:

Bit7-0	REV2
-	Increased each revision

R80H(AMV): Auto Measurement VCOM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
AMV	W	0	1	0	0	0	0	0	0	0	(80H)
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	AMVX	AMVS	AMV	AMVE	(00H)

This command indicates the IC status.Host can read this data to understand the IC status.

This command only active when BUSY_N="1"

1st Parameter:

Bit7-6	The sensing points of sampling time
00	2(default)
01	4
10	8
11	16

Sampling time= the last quarter of sensing time (T)

VCOM = average of N points. N=2,4,8,16

Bit5-4	The sensing time of VCOM detection
00	5s(default)
01	10s
10	15s
11	20s

Bit3	XON setting for all Gate ON of AMV
0	Gate scan normally during Auto Measure VCOM period.(default)
1	All Gate ON during Auto Measure VCOM period.

Bit2	AMVS setting for Source output of AMV
0	Source output 0V during Auto Measure VCOM period.(default)
1	Source output VSPL during Auto MeasureVCOM period.

Bit1	Analogy signal
0	Get VCOM value by R81H(default)
1	Gate scan only. Measure VCOM externally by probing the VCOM pad.

Bit0	Auto Measure VCOM setting
0	Auto measure VCOM disble (default)
1	Auto measure VCOM enable

R81H(VV): VCOM Value Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VV	W	0	1	0	0	0	0	0	0	1	(81H)
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	(00H)

This command gets Vcom value.

1st Parameter:

Bit6-0	VCOM value
0000000	0V
0000001	-0.05V
0000010	-0.10V
⋮	⋮
1010000	-4.00V
Others	-4.00V

R82H(VDCS): VCM_DC Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VDCS	W	0	1	0	0	0	0	0	1	0	(82H)
1st Parameter	W	1	OTP_VCM	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	(00H)

This command set the VCOMDC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit7	Follow OTP VCOM value in OTP mode
0	IP output value(default)
1	From the setting register

Bit6-0	VCOM value
0000000	0V(default)
0000001	-0.05V
0000010	-0.10V
⋮	⋮
1010000	-4.00V
Others	-4.00V

R90H(PGM): Program Mode

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Ente rProgram Mode	W	0	1	0	0	1	0	0	0	0	(90H)

After this command is issued,the chip would enter the program mode.

After the programming procedure completed,a hardware reset is necessary for leaving program mode

R91H(APG): Active Program

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Active Program OTP	W	0	1	0	0	1	0	0	0	1	(91H)

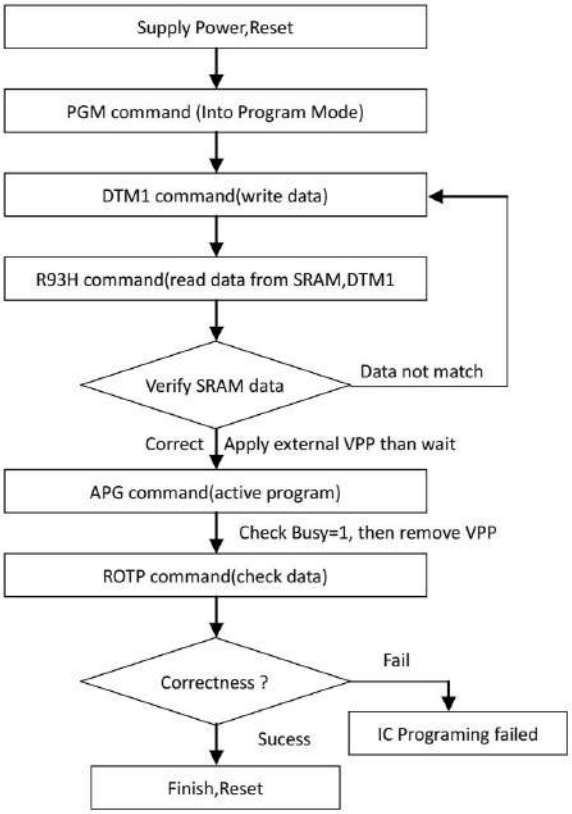
After this command is transmitted,the programming state machine would be activated.

The BUSY_N flag would fall to 0 until the programming is completed.

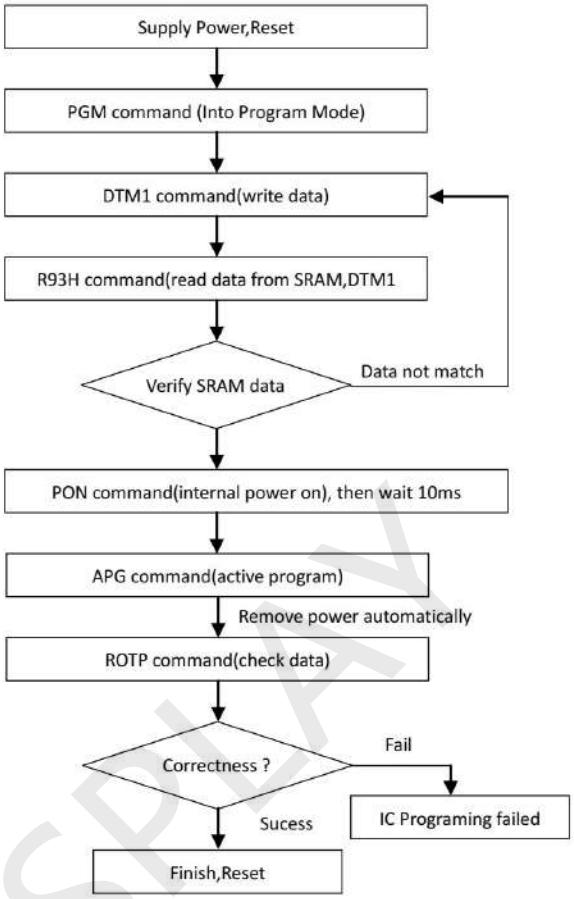
This command only active when BUSY_N="1"

R92H(ROTP): Read OTP Data

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read OTP Data	W	0	1	0	0	1	0	0	1	0	(92H)
	R	1	Dummy								(00H)
	R	1	The data of address0 in the OTP								(00H)
	R	1									(00H)
	R	1	The data of address(n) in the OTP								(00H)



OTP Programming Flow (External VPP)



OTP Programming Flow (Internal VPP)

R93H(RSRAM):Read SRAM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read SRAM Data	W	0	1	0	0	1	0	0	1	1	(93H)
	R	1	Dummy								(00H)
	R	1	The data of address0 in the SRAM								(00H)
	R	1									(00H)
	R	1	The data of address(n) in the SRAM								(00H)

RA2H(PGM_CFG):OTP Program Config Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP program Config	W	0	1	0	1	0	0	0	1	0	(A2H)
1st Parameter	W	1	-	-	-	VPPSEL	-	-	**M_dis**	**S_dis**	(00H)
2nd Parameter	W	1	PGM_SADDR[15:8]								(00H)
3rd Parameter	W	1	PGM_SADDR[7:0]								(00H)
4th Parameter	W	1	PGM_DSIZE[15:8]								(15H)
5th Parameter	W	1	PGM_DSIZE[7:0]								(DFH)

This command is to set the configuration of OTP

1st Parameter

Bit4	VPPSEL
0	External VPP **(default)**
1	Internal VPP

Bit1	M_dis
0	Enable specific command **(default)**
1	Disable specific command

Enable/Disable some command when IC sets Master (MS Pin is High).

Bit0	S_dis
0	Enable specific command **(default)**
1	Disable specific command

Enable/Disable some command when IC sets Slave (MS Pin is Low).

***Notes: Specific command define: R00H(Parameter 1)(PSR), R10H(DTM), R90H(PGM), R91H(APG), R83H(PTLW)**

***For command reading, only the bit of M_dis or S_dis can be set to 1.**

2nd and 3rd Parameters: Program start address PGM_SADDR[15:0]

4th and 5th Parameters: Program data size PGM_SADDR[15:0]

Default PGM_DSIZE[15:0] is 0x15DF.

RA3H(PGM_STAT):OTP Program Status Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP program Status	W	0	1	0	1	0	0	0	1	1	(A3H)
1st Parameter	W	1	-	-	-	-	-	-	PGM_VER_ERR	PGM_EXE_ERR	(00H)

This command is to read OTP Program status

1st Parameter:

Bit1	Data verification of APG
0	OK
1	NOK

Bit0	OTP program execution status
0	Normal
1	Invalid APG setting

RE0H(CCSET):Chip Temperature Input Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Temperature Input	W	0	1	1	1	0	0	0	0	0	(E0H)
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	**CCEN**	(00H)

This command is control input path of temperature value

1st Parameter:

Bit0	Output clock enable/disable
0	Output 0v at CL pin **(default)**
1	Ouptut clock at CL pin for alave chip.**(Cascade mode)**

CCEN=1 : The master temperature is synchronized with the salve. This setting needs to wait until BUSY_N="1".

Bit1	Temperature Input Selection
0	Use temperature sensor **(default)**
1	Use TSSET[7:0] value

RE4H(LVSEL): LVD Voltage Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Select LVD Voltage	W	0	1	1	1	0	0	1	0	0	(E4H)
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		(03H)

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVDvalue
00	<2.2V
01	<2.3V
10	<2.4V
11	<2.5V (default)

RE6H(TSSET): Force Temperature Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Force Temperature	W	0	1	1	1	0	0	1	1	0	(E6H)
1st Parameter	W	1	TS[7]	TS[6]	TS[5]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]	(03H)

TS[7:0]: Temperature boundary: -25C~60C

When TSFIX=1, Internal TS is disable, Temperature value will be set by TS[7:0].

TS[7:0]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
…	…
1111_1110	-2
1111_1111	-1

TS[7:0]	Temperature (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
…	…
0011_1011	59
0011_1100	60

RFFH(TEST): Enter TEST MODE

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	1	1	(FFH)
1st Parameter	W	1	1	0	1	0	0	1	0	1	(A5H)

TEST(0xFF)+Code(0xA5)=Enter TEST MODE

RFFH(TEST): Exit TEST MODE

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	1	1	(FFH)
1st Parameter	W	1	1	1	1	0	0	0	1	1	(E3H)

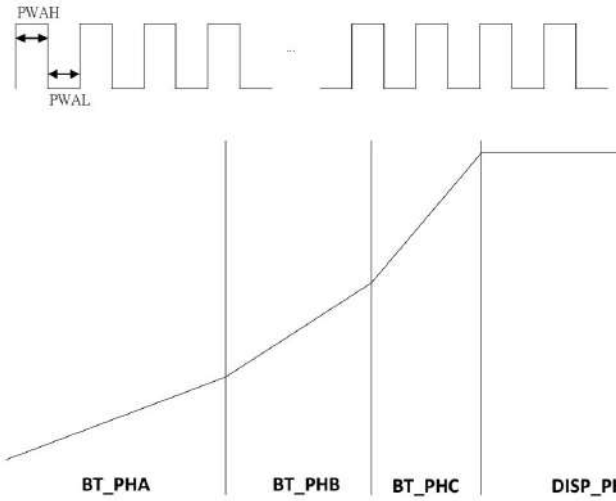
TEST(0xFF)+Code(0xE3)=Exit TEST MODE

REFH(TEST): POWER PWM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	1	1	1	(EFH)
1st Parameter	W	1	BT_PWAH								(01H)
2st Parameter	W	1	BT_PWAL								(03H)
3st Parameter	W	1	BT_PWBH								(03H)
4st Parameter	W	1	BT_PWBL								(10H)
5st Parameter	W	1	BT_PWCH								(04H)
6st Parameter	W	1	BT_PWCL								(20H)
7st Parameter	W	1	DISP_PWDH								(06H)
8st Parameter	W	1	DISP_PWDL								(20H)

1nd Parameter:

Bit7-0	PWxH/L time
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns



1st、2nd parameter : correspond to the PWM duty cycle within a specified time for the R06H command BT_PHA.

3rd、4th parameter : correspond to the PWM duty cycle within a specified time for the R06H command BT_PHB.

5th、6th parameter : correspond to the PWM duty cycle within a specified time for the R06H command BT_PHC.

7th、8th parameter : the PWM duty cycle within display refresh(DISP_PHD).

RC9H(TEST): GDROTP

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	0	1	0	0	1	(C9H)
1st Parameter	W	1	GDR_OTP_R								(F8H)

Adjust the GDR driving for the three-stage voltage boosting during POWER ON and display refresh.

Bit7-6	GDR driving within DISP_PHD
Bit5-4	GDR driving within BT_PHC
Bit3-2	GDR driving within BT_PHB
Bit1-0	GDR driving within BT_PHA

RDAH(TEST): Driving Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	0	1	0	(DAH)
1st Parameter	W	1	-	-	VRES_SEL		1	-	-	-	(08H)

Adjust the VDDL driving

Bit5-4	VDDL driving	00:weak 11:strong

RDBH(TEST): CPCK_ SEL

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	0	1	1	(DBH)
1st Parameter	W	1	0	0	0	0	0	0	CPCK_SEL		(03H)

CPCK_SEL	00:8Mhz, 01:1Mhz, 10:2Mhz, 11:4Mhz(default)

RDCH(TEST): CPCK SET enable

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	0	(DCH)
1st Parameter	W	1	0	0	0	0	0	0	CPCKDF EN	CPCKEN	(03H)

Bit0	CPCK enable 0:OFF 1:ON
Bit1	CPCKDFEN :CPCK PWH SET & CPCK PWL SET enable 1:follow default 0:follow RDDH & RDEH

RDDH(TEST): CPCK PWH SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	1	(DDH)
1st Parameter	W	1	CPCK PWH SET								(08H)

Adjust the sampling frequency of VDH/VDL/VDHR clamping.

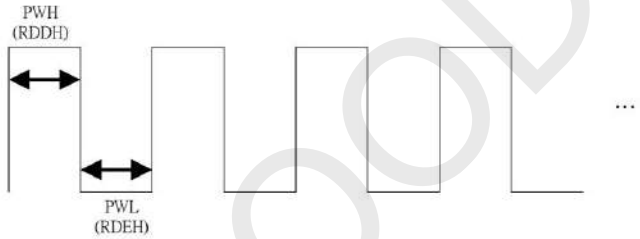
Bit7-0	CPCK PWH SET	Bit7-0	CPCK PWH SET
00H	0 ns	:	:
01H	125 ns	FCH	31500ns
02H	250 ns	FDH	31625ns
03H	375 ns	FEH	31750ns
04H	500 ns	FFH	31875ns

RDEH(TEST): CPCK PWL SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	1	0	(DEH)
1st Parameter	W	1	CPCK PWL SET								(08H)

Adjust the sampling frequency of VDH/VDL/VDHR clamping.

Bit7-0	
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns



RDFH(TEST): VD_Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	1	1	(DFH)
1st Parameter	W	1	0	0	VDHR_SEL		VDH_SEL		VDL_SEL		(3FH)

Bit5-4	VDHR driving	00:weak	11:strong
Bit3-2	VDH driving	00:weak	11:strong
Bit1-0	VDL driving	00:weak	11:strong

RA8H(TEST): VDHROS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	0	1	0	1	0	0	0	(A8H)
1st Parameter	W	1	0	0	1	1	1	1	1	VDHROS EN	(3FH)

Adjust the compensation driving of VDHR, which affects the waveform during VDHR switching.

Bit0	VDHR driving enable
0	VDHR driving OFF
1	VDHR driving ON(default)

RE8H(TEST): VDLOS_Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	0	0	0	(E8H)
1st Parameter	W	1	0	0	0	0	0	0	VDLOS_SEL		(01H)

Adjust the compensation driving of VDL, which affects the waveform during VDL switching.

Bit1-0	Adjusting VDL driving 00: strong 11:weak

RFDH(TEST): VDLOS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	0	1	(FDH)
1st Parameter	W	1	0	0	0	0	0	0	0	VDLOS EN	(00H)

Bit0	VDL compensation driving enable
0	VDL compensation driving OFF(default)
1	VDL compensation driving ON

8. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color(black, white, red and yellow) Good Display 's E-pa per Display. And it is also added the functions of USB serial port, FLASH c hip, font chip, current detection ect.
Development Kit consists of the development board and the pinboard.

Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc. More details, please click to the following links:

STM32 https://www.good-display.com/product/219.html

ESP32 https://www.good-display.com/product/338.html

ESP8266 https://www.good-display.com/product/220.html

Arduino UNO https://www.good-display.com/product/222.html

9. Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detectionis perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
T update	Image update time	at 25 °C		26	-	sec	
Life		Topr		1000000times or 5years			

Notes: Luminance meter: Eye-One Pro Spectrophotometer.
8-1.8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

10. Handling, Safety and Environment Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

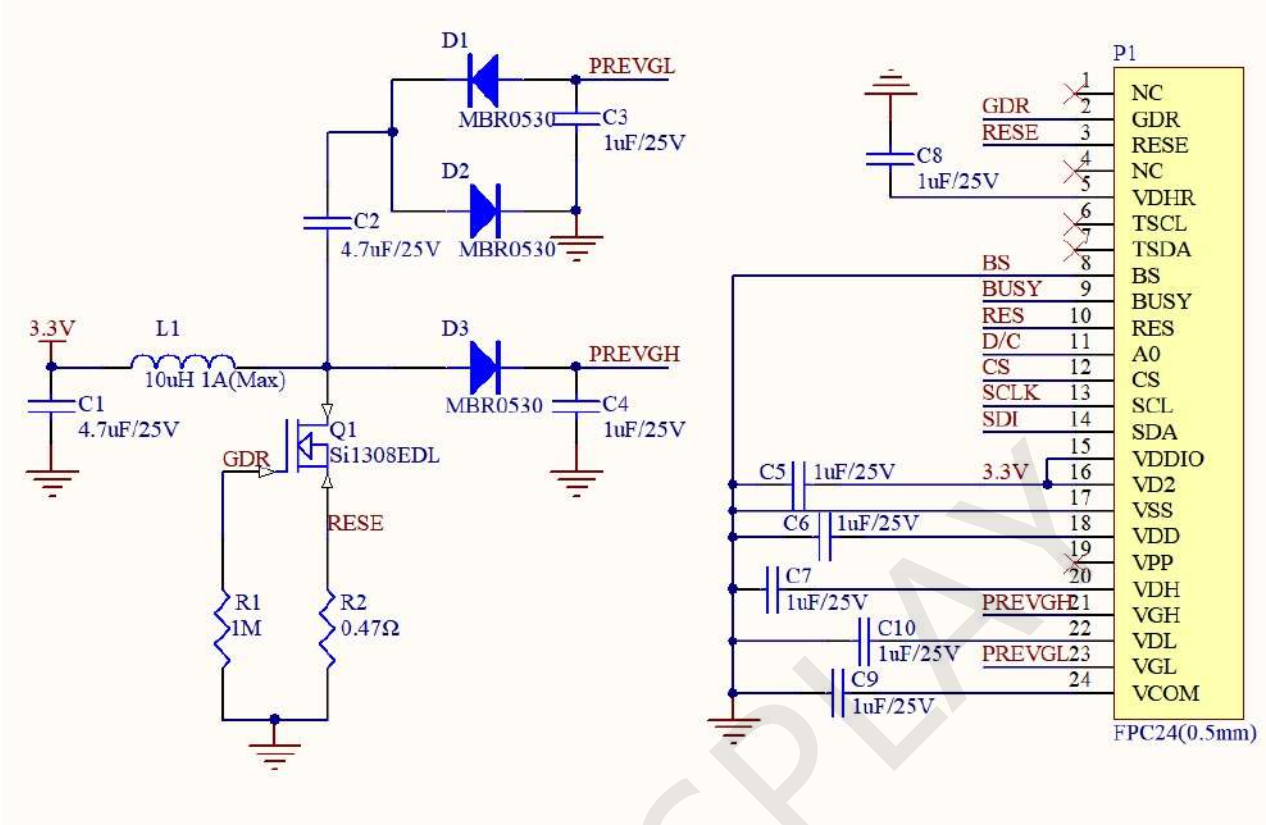
Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

11.Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60° C，RH=35%，240h Test in white pattern
3	High-Temperature Operation	T=40° C，RH=35%，240h
4	Low-Temperature Operation	T= 0° C，240h
5	High-Temperature, High-Humidity Operation	T=40° C，RH=80%，240h
6	High Temperature, High Humidity Storage	T=50° C，RH=90%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25℃ 30min]→[+60℃ 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

12.Circuit Drawing



13. Inspection method and condition

13.1 Inspection condition

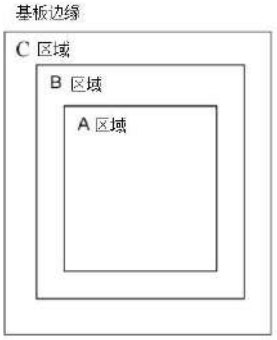
Item	Condition
Illuminance	800~1500 lux
Temperature	22℃ ±3℃
Humidity	55±10 %RH
Distance	≥30cm
Angle	Vertical fore and aft 45
Inspection method	By eyes

13.2 Zone definition

A Zone： Active area

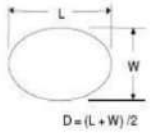
B Zone： Border zone

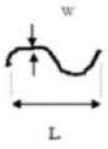
C Zone： From B zone edge to panel edge

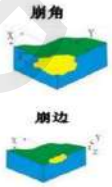
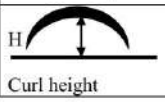


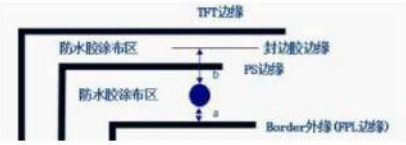
13.3 General inspection standards for products

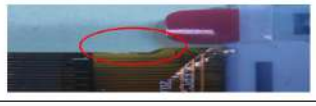
13.3.1 Appearance inspection standard

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Spot defects	Spot defects such as dot, foreign matter, air bubble, and dent etc.	Diameter D=(L+W)/2 (L-length、W-width) Measuring method shown in the figure below 	The distance between the two spots should not be less than 10mm	7.5"-13.3"Module（Not include 7.5"）： D＞1mm N=0 0.5＜D≤0.8 N≤4 D≤0.5 Ignore 0.8＜D≤1 N≤2 4.2"-7.5"Module（Not include 4.2"）： D＞0.5 N=0 0.4＜D≤0.5 N≤2 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 Module below 4.2"： D＞0.5 N=0 0.4＜D≤0.5 N≤1 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 0.1mm＜D≤0.25 N≤3/cm²	Foreign matter D≤1mm Pass	Check by eyes Film gauge	MIN

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Line defects	Line defects such as scratch, hair etc.	L-Length，W-Width，(W/L)＜1/4 Judged by line， (W/L)≥1/4 Judged by dot 	The distance between the two lines should not be less than 5mm	7.5"-13.3"Module（Not include 7.5"）： L＞10mm,N=0 W＞0.8mm，N=0 5mm≤L≤10mm，0.5mm≤W≤0.8mm N≤2 L≤5mm，W≤0.5mm Ignore 4.2"-7.5"Module（Not include 4.2"）： L＞8mm,N=0 W＞0.2mm，N=0 2mm≤L≤8mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore Module below 4.2"： L＞5mm,N=0 W＞0.2mm，N=0 2mm≤L≤5mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore	Ignore	Check by eyes Film gauge	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Panel chipping and crack defects	TFT panel chipping	X the length, Y the width, Z the chipping height, T the thickness of the panel 	Chipping at the edge： Module over 7.5"（Include 7.5"）： X≤6mm,Y≤1mm Z≤T N=3 Allowed Module below 7.5"(Not include 7.5")： X≤3mm,Y≤1mm Z≤T N=3 Allowed Chipping on the corner： IC sideX≤2mm Y≤2mm, Non-IC sideX≤1mm Y≤1mm . Allowed Note： Chipping should not damage the edge wiring. If it does not affect the display, allowed	Check by eyes、 Film gauge	MIN
	Crack		Crack at any zone of glass , Not allowed	Check by eyes、Film gauge	MIN
	Burr edge		No exceed the positive and negative deviation of the outline dimensions X+Y≤0.2mm Allowed	Calliper	MIN
	Curl of panel	 Curl height	Curl height H≤Total panel length 1% Allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ / MIN
PS defect	Water proof film		1 .Waterproof film damage, wrinkled, open edge, not allowed 2. Exceeding the edge of module(according to the lamination drawing) Not allowed 3. Edge warped exceeds height of technical file, not allowed	Check by eyes	MIN
RTV defect	Adhesive effect		Adhesive height exceeds the display surface, not allowed	Check by eyes	MIN
			1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2 .No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3. No adhesive at edge and corner1*1mm, no exposure of wiring, allowed		
			Protection adhesive, coverage width within W≤1.5mm, no break of adhesive, allowed		
	Adhesive re-fill		Dispensing is uniform, without obvious concave and breaking, bubbling and swell, not higher than the upper surface of the PS, and the diameter of the adhesive re-filling is not more than 8mm, allowed	Check by eyes	MIN
EC defect	Adhesive bubble		1、 Effective edge sealing area of hot melt products ≥1/2 edge sealing area; 2、Bubble a+b≥1/2 effective width, N≤3, spacing≥5mm , allowed No exposure of wiring, allowed	Check by eyes	MIN

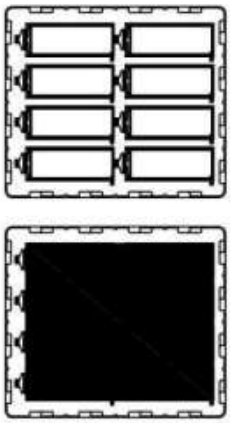
Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
EC defect	Adhesive effect		1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2.No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3.No adhesive at edge and corner 1*1mm, no exposure of wiring, allowed 4. Adhesive height exceeds the display surface, not allowed	Visual, caliper	MIN
Silver dot adhesive defect	Silver dot adhesive		1、Single silver dot dispensing amount ≥1mm, allowed 2、One of the double silver dot dispensing amount is ≥1mm and the other has adhesive (no reference to 1mm) Allowed	Visual	MIN
			Silver dot dispensing residue on the panel ≤0.2mm, allowed	Film gauge	MIN
FPC defect	FPC wiring FPC golden finger		FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
			The height of burr edge of TCP punching surface ≧ 0.4mm, not allowed	Caliper	MIN
	FPC damage/crease		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Protective film defect	Protective film	Scratch and crease on the surface but no affect to protection function, allowed		Check by eyes	MIN
		Adhesive at edge L≤5mm，W≤0.5mm，N=2, no entering into viewing area		Check by eyes	MIN
Stain defect	Stain	If stain can be normally wiped clean by > 99% alcohol, allowed		Visual	MIN
Pull tab defect	Pull tab	The position and direction meet the document requirements, and ensure that the protective film can be pulled off.		Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape	Tilt≤10°, flat without warping, completely covering the IC.		Check by eyes/ Film gauge	MIN
Stiffener	Stiffener	Flat without warping, Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than 0.5mm from FPC edge		Check by eyes	MIN
Label	Label/ Spraying code	The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.		Check by eyes	MIN

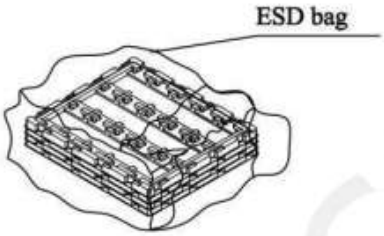
14. Packaging

PACKLING ORDER:

1) Putting 8 pcs Modules on each PET tray.And cover a dedicated EPE film.

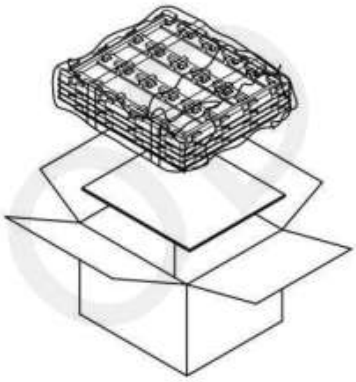


2) Putting 22 pcs PET trays together with 1 empty tray on the top of PET tray. Insert in the ESD bag, add desiccant in the ESD bag.

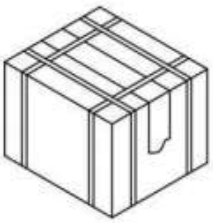


3) the tray together with adhesive tape

4) Putting into one outcarton



5) Packing finished



Note:8 pcs in a tray, 22 trays in a out carton, so 8*22=176 pcs/Outcarton

Dimension (Out carton): 510*360*215㎜

15. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.(4)

Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores theESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPDpanel's performance. Please do not expose the unprotected EPD panel to hightemperature, high humidity, sunlight, or fluorescent for long periods of time.

https://www.good-display.com/news/80.html