



# 4.2 inch E-paper Display Series

## **GDEM042F52**



Dalian Good Display Co., Ltd.

# Product Specifications



<b>Customer</b>	<b>Standard</b>
<b>Description</b>	<b>4.2" E-PAPER DISPLAY</b>
<b>Model Name</b>	<b>GDEM042F52</b>
<b>Date</b>	<b>2024/06/17</b>
<b>Revision</b>	<b>1.0</b>

	Design Engineering		
	Approval	Check	Design
			

No.18, Zhonghua West ST,Ganjingzi DST,Dalian,CHINA

Tel: +86-411-84619565

Email: info@good-display.com

Website: www.good-display.com

---

# CONTENTS

1. Over View .....	4
2. Features .....	4
4. Mechanical Drawing of EPD Module .....	5
5. Input/output Pin Assignment .....	6
6. Electrical Characteristics .....	8
7. Command Table .....	12
8. Block Diagram .....	46
9. Typical Application Circuit with SPI Interface .....	47
10 Typical Operating Sequence .....	49
11. Reliability Test .....	50
12. Quality Assurance .....	51
13. Mated Development Kit .....	55
14. Handling, Safety, and Environment Requirements .....	56
15. Packaging .....	57
16. Precautions .....	58

## 1. Over View

GDEM042F52 is an Active Matrix E Ink Display all-in-one driver with timing controller for ESL. The sources have 2-bit outputs per pixel to support white/black/red/yellow. The 4.2 inch active area contains 400×300 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

## 2. Features

- ◆400×300 pixels display
- ◆High contrast High reflectance
- ◆Ultra wide viewing angle Ultra low power consumption
- ◆Pure reflective mode
- ◆Bi-stable display
- ◆Commercial temperature range
- ◆Landscape portrait modes
- ◆Hard-coat antiglare display surface
- ◆Ultra Low current deep sleep mode
- ◆On chip display RAM
- ◆Waveform can stored in On-chip OTP or written by MCU
- ◆Serial peripheral interface available
- ◆On-chip oscillator
- ◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆I<sup>2</sup>C signal master interface to read external temperature sensor
- ◆Built-in temperature sensor

### 4. Mechanical Drawing of EPD Module

Confirmation:	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 20%;">DATE</th> <th style="width: 20%;">REV.</th> <th style="width: 60%;">MODIFICATION</th> </tr> <tr> <td style="text-align: center;">2023-09-03</td> <td style="text-align: center;">A</td> <td style="text-align: center;">FIRST ISSUE</td> </tr> </table>	DATE	REV.	MODIFICATION	2023-09-03	A	FIRST ISSUE																												
DATE	REV.	MODIFICATION																																	
2023-09-03	A	FIRST ISSUE																																	
<p>FRONT VIEW</p>	<p>SIDE VIEW</p>	<p>BACK VIEW</p>																																	
<p>NOTE</p> <ol style="list-style-type: none"> <li>1 DISPLAY MODULE 4.2" ARRAY FOR EPD</li> <li>2 DRIVER IC: JD79668</li> <li>3 RESOLUTION: 300gateX400source</li> <li>4 PIXEL SIZE: 0.212mmX0.212mm</li> </ol>		<p><b>Dalian Good Display Co., Ltd.</b></p>																																	
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20%;">TOLERANCES UNMARKED</td> <td style="width: 15%;">TITLE: EPD</td> <td style="width: 15%;">PROJECT: GDEM042F52</td> <td style="width: 10%;">REV: A</td> <td style="width: 10%;">DATE: 23.09.03</td> <td style="width: 30%;">CUST. P/N:</td> </tr> <tr> <td>ANGLES ±5°</td> <td>DWN: NN ZHAO</td> <td>CHK: CC ZHENG</td> <td>APPR: LY YU</td> <td>UNIT: mm</td> <td>PAGE: 1/1</td> </tr> <tr> <td>.X = ±0.4mm</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>.XX = ±0.20mm</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>.XXX = ±0.20mm</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </table>	TOLERANCES UNMARKED	TITLE: EPD	PROJECT: GDEM042F52	REV: A	DATE: 23.09.03	CUST. P/N:	ANGLES ±5°	DWN: NN ZHAO	CHK: CC ZHENG	APPR: LY YU	UNIT: mm	PAGE: 1/1	.X = ±0.4mm						.XX = ±0.20mm						.XXX = ±0.20mm										
TOLERANCES UNMARKED	TITLE: EPD	PROJECT: GDEM042F52	REV: A	DATE: 23.09.03	CUST. P/N:																														
ANGLES ±5°	DWN: NN ZHAO	CHK: CC ZHENG	APPR: LY YU	UNIT: mm	PAGE: 1/1																														
.X = ±0.4mm																																			
.XX = ±0.20mm																																			
.XXX = ±0.20mm																																			

## 5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC		Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	NC		Do not connect with other NC pins	Keep Open
7	NC		Do not connect with other NC pins	Keep Open
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

**I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin**

**Note 5-1:** This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

**Note 5-2:** This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

**Note 5-3:** This pin (RES#) is reset signal input. The Reset is active low.

**Note 5-4:** This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin Low when -Outputting display waveform -Communicating with digital temperature sensor

**Note 5-5:** Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

## 6. Electrical Characteristics

### 6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.3 to +6.0	V
Logic Input voltage	VIN	-0.3 to VCI +0.3	V
Operating Temp range	TOPR	0 to +40	°C.
Storage Temp range	TSTG	-25 to+70	°C.
Optimal Storage Humidity	HST Go	55±10	%RH

**Note:**

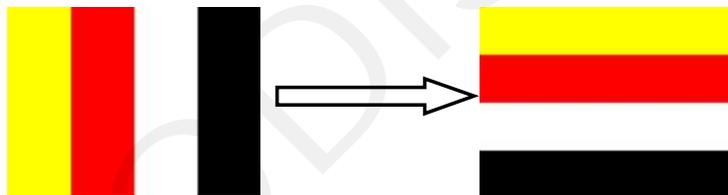
1. Maximum ratings are those values beyond which damages to the device may occur.Functional operation should be restricted to the limits in the Panel DC Characteristics tables.
2. The storage time is within 10 days for -25°C ~ 70°C.  
The display screen should be kept white and face up.

## 6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	VSS	-		-	0	-	V
Logic supply voltage	VCI	-	VCI	2.3	3.3	3.6	V
Core logic voltage	VDD		VDD	2.3	3.3	3.6	V
High level input voltage	V <sub>IH</sub>	-	-	0.7 VCI	-	VCI	V
Low level input voltage	V <sub>IL</sub>	-	-	0	-	0.3 VCI	V
High level output voltage	V <sub>OH</sub>	IOH = 400Ma	-	VCI -0.4	-	-	V
Low level output voltage	V <sub>OL</sub>	IOL = -400Ma	-	-	-	GND +0.4	V
Typical power	P <sub>TYP</sub>	VCI =3.0V	-	-	18.6	-	mW
Deep sleep mode	P <sub>STPY</sub>	VCI =3.0V	-	-	0.0012	-	mW
Typical operating current	I <sub>opr_VCI</sub>	VCI =3.0V	-	-	6.2	-	mA
Full/Fast update time	-	23 °C	-	-	20/12	-	sec
Deep sleep mode current	I <sub>dslp_VCI</sub>	DC/DC off No clock No input load Ram data not retain	-	-	0.4	1	uA

Notes: 1. The typical power is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern.



- The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display
- Electrical measurement: Tektronix oscilloscope - MDO3024,  
Tektronix current probe–TCP0030A.

### 6.3 Panel AC Characteristics

#### 6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
	SDA	SCL	CS#	D/C#	RES#
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

**Table 6-3-1: MCU interface assignment under different bus interface mode**

#### 6.3.2 MCU Serial Interface (4-wire SPI)

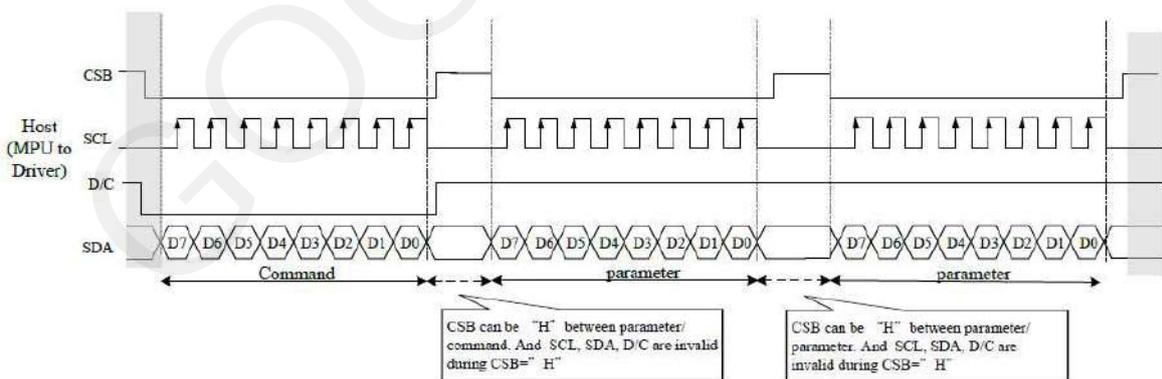
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

**Table 6-3-2: Control pins of 4-wire Serial Peripheral interface**

Note: ↑ stands for rising edge of signal

**Figure 6-3-1: 4-wire SPI mode**



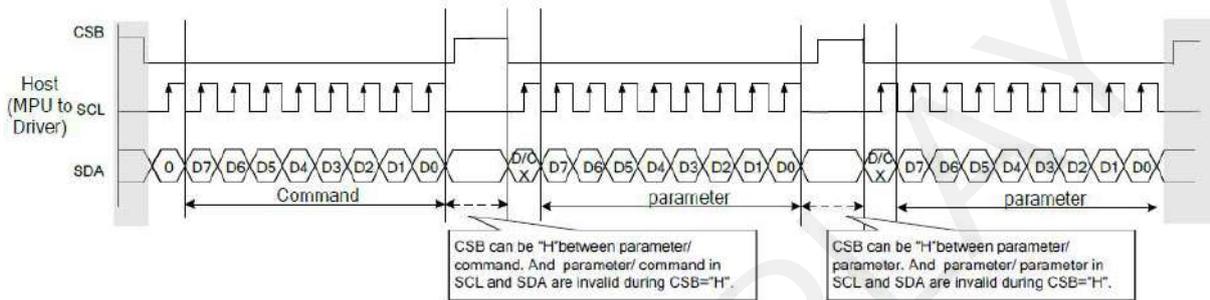
### 6.3.3 MCU Serial Interface (3-wire SPI)

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

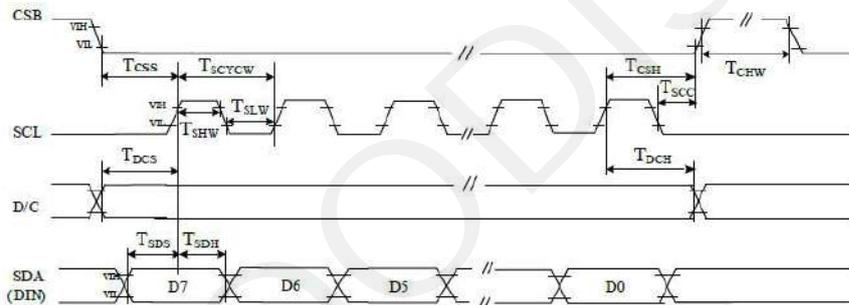
Table 6-3-3: Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

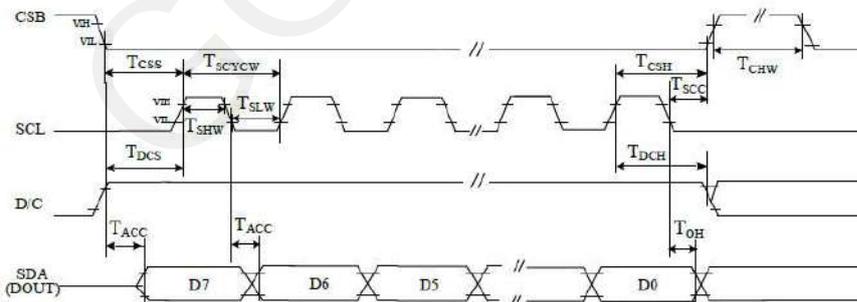
Figure 6-3-2: 3-wire SPI mode



### 6.3.4 Interface Timing



4 pin serial interface characteristics(write mode)



**Serial Interface Timing Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>SERIAL COMMUNICATION</b>						
CSB	$T_{CSS}$	60			ns	Chip select setup time
	$T_{CSH}$	65			ns	Chip select hold time
	$T_{SCC}$	20			ns	Chip select CSB setup time
	$T_{CHW}$	40			ns	Chip select setup time
SCL	$T_{SCYCW}$	100			ns	Serial clock cycle (Write)
	$T_{SHW}$	35			ns	SCL "H" pulse width (Write)
	$T_{SLW}$	35			ns	SCL "L" pulse width (Write)
	$T_{SCYCR}$	150			ns	Serial clock cycle (Read)
	$T_{SHR}$	60			ns	SCL "H" pulse width (Read)
	$T_{SLR}$	60			ns	SCL "L" pulse width (Read)
SDA (DIN) (DOUT)	$T_{SDS}$	30			ns	Data setup time
	$T_{SDH}$	30			ns	Data hold time
	$T_{ACC}$			10	ns	Access time
	$T_{OH}$	15			ns	Output disable time
D/C	$T_{DCS}$	20			ns	DC setup time
	$T_{DCH}$	20			ns	DC hold time

## 7.Command Table

### Register Table

Following table list all the SPI control registers and bit name definition for JD79668. Refer to the next section for detail register function description.

Address	command	Bit										Code
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00h
		W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
		W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	-	V8C_EN	V8S_EN	V8G_EN	07h
		W	1	-	-	-	-	-	-	V8PN [1]	V8PN [0]	00h
		W	1	-	V8PL_0[6]	V8PL_0[5]	V8PL_0[4]	V8PL_0[3]	V8PL_0[2]	V8PL_0[1]	V8PL_0[0]	00h
		W	1	-	V8P_1[5]	V8P_1 [5]	V8P_1 [4]	V8P_1 [3]	V8P_1 [2]	V8P_1 [1]	V8P_1 [0]	00h
		W	1	-	V8N_1[5]	V8N_1[5]	V8N_1[4]	V8N_1[3]	V8N_1[2]	V8N_1[1]	V8N_1[0]	00h
		W	1	-	V8PL_1[5]	V8PL_1[5]	V8PL_1[4]	V8PL_1[3]	V8PL_1[2]	V8PL_1[1]	V8PL_1[0]	00h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
		W	1	-	-	-	-	-	-	-	-	00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	-	-	-	-	PHE_SFT[1:0]		PHA_SFT[1:0]		00h
		W	1	-	-	-	-	PHA_ON[5:0]				02h
		W	1	-	-	-	-	PHA_OFF[5:0]				07h
		W	1	-	-	-	-	PHB_ON[5:0]				02h
		W	1	-	-	-	-	PHB_OFF[5:0]				07h
		W	1	-	-	-	-	PHC_ON[5:0]				02h
W	1	-	-	-	-	PHC_OFF[5:0]				07h		
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	ASh
R10H	Data Start transmission (DTM)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00h
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	-
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
		W	1	-	-	-	-	-	-	-	-	00h
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	ASh
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	-	-	-	Dyna		FR[2:0]		02h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/T8[7]	D9/T8[7]	D8/T8[6]	D7/T8[5]	D6/T8[4]	D5/T8[3]	D4/T8[2]	D3/T8[1]	--
R41H	Temperature Sensor Calibration (TSE)	R	1	D2/T8[9]	D1/T8[8]	D0	-	-	-	-	-	--
		W	0	0	1	0	0	0	0	0	1	41H
R42H	Temperature Sensor Write (TSW)	W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h
		W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
R43H	Temperature Sensor Read (TSR)	W	1	WM8B[7]	WM8B[6]	WM8B[5]	WM8B[4]	WM8B[3]	WM8B[2]	WM8B[1]	WM8B[0]	00h
		W	1	WL8B[7]	WL8B[6]	WL8B[5]	WL8B[4]	WL8B[3]	WL8B[2]	WL8B[1]	WL8B[0]	00h
		W	0	0	1	0	0	0	0	1	1	43H
R43H	Temperature Sensor Read (TSR)	R	1	RM8B[7]	RM8B[6]	RM8B[5]	RM8B[4]	RM8B[3]	RM8B[2]	RM8B[1]	RM8B[0]	--
		R	1	RL8B[7]	RL8B[6]	RL8B[5]	RL8B[4]	RL8B[3]	RL8B[2]	RL8B[1]	RL8B[0]	--

R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H	
		W	1	VBD[2]	VBD[1]	VBD[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h	
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H	
		R	1	-	-	-	-	-	-	-	LPD	--	
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H	
		W	1	-	-	-	-	-	-	HRES[9]	HRES[8]	00h	
		W	1	HRES[7]	HRES[6]	HRES[5]	HRES[4]	HRES[3]	HRES[2]	0	0	00h	
		W	1	-	-	-	-	-	-	VRES[9]	VRES[8]	00h	
		W	1	VRES[7]	VRES[6]	VRES[5]	VRES[4]	VRES[3]	VRES[2]	VRES[1]	VRES[0]	00h	
R65H	Gate/Source Start Setting(GSST)	W	0	0	1	1	0	0	1	0	1	65H	
		W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h	
		W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h	
		W	1	-	-	-	gsCan	-	-	G_start[9]	G_start[8]	00h	
		W	1	G_start[7]	G_start[6]	G_start[5]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h	
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H	
		R	1	0	0	0	0	0	0	1	1	06h	
		R	1	0	0	0	0	0	0	1	0	02h	
		R	1	0	0	0	0	0	0	0	1	01h	
R80H	Auto Measure Voom (AMV)	W	0	1	0	0	0	0	0	0	0	80H	
		W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMV3	AMV	AMVE	00h	
R81H	Voom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H	
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--	
R82H	Voom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H	
		W	1	-	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h	
R83H	Partial Window (PTLW)	W	0	1	0	0	0	0	0	1	1	83H	
		W	1	-	-	-	PTH_ENB	-	-	HRST[9]	HRST[8]	00h	
		W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	0	0	00h	
		W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h	
		W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	0	0	00h	
		W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h	
		W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h	
		W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h	
		W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h	
		W	1	-	-	-	-	-	-	-	P.MODE	00h	
R90H	Program mode(PGM)	W	0	1	0	0	1	0	0	0	0	90H	
R91H	Active Program(APG)	W	0	1	0	0	1	0	0	0	1	91H	
R92H	Read MTP data (RMTP)	W	0	1	0	0	1	0	0	1	0	92H	
		R	1	#	#	#	#	#	#	#	#	-	
RA2H	MTP Program Config Register(PGM_CFG)	W	0	1	0	1	0	0	0	1	0	A2H	
		W	1	-	-	-	VMTPSEL	-	-	M_dis	S_dis	00h	
		W	1	PGM_SADDR[16:8]									00h
		W	1	PGM_SADDR[7:0]									00h
		W	1	PGM_DSIZE[16:8]									0Fh
W	1	PGM_DSIZE[7:0]									00h		
RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H	
		W	1	-	-	-	-	-	-	-	CCEIN	00h	
RE3H	Power saving(PWS)	W	0	1	1	1	0	0	0	1	1	E3H	
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[1]	SD_W[0]	00h	
RE4H	LVD voltage Select(LVSEL)	W	0	1	1	1	0	0	1	0	0	E4H	
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h	

R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1 <sup>st</sup> Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2 <sup>nd</sup> Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as :		
	1 <sup>st</sup> parameter		
	Bit	Name	Description
	0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating
	1	SHD_N	SHD_N function 0: Booster OFF, register data are kept, and Source / Border / Vcom are kept 0V or floating. 1: Booster on. (default)
	2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →...→S2→Last data=S1. 1: Shift right; First data=S1→S2 →...→Sn-1→Last data=Sn. (default)
	3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →...→G2→Last line=G1. 1:Scan up; First line=G1→G2 →...→Gn-1→Last line=Gn. (default)
	5	PST_MODE	Power switch operation mode 0:Power switching time in the period of frame scanning.(default) 1:Power switching time in the external period before frame scanning.
7-6	RES[1,0]	Resolution setting 00: Display resolution is 400x300(default) 01: Display resolution is 320x300 10: Display resolution is 300x240 11: Display resolution is 200x300	

2 <sup>nd</sup> parameter		
Bit	Name	Description
0	VC_LUTZ	VCOM status function 0 : No effect 1 : After refreshing display, the output of VCOM is set to floating automatically (default)
1	NORG	VCOM status function 0 : No effect (default) 1 : After refreshing display, VCOM is tied to GND before power off
2	TIEG	VGN power off status function 0 : No effect (default) 1 : Power off, VGN will be tied to GND
3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling booster, Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high, Temperature Sensor will be activated automatically one time. (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	FOPT	FOPT function 0 : Scan 1 frame after waveform finished(default) 1 : No scan after waveform finished and switch the source channel output to Hiz.
7	LUT_EN	LUT selection setting 0 : Using LUT from MTP(default) 1 : Using LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC\_LUTZ

FOPT setting is part of refreshing display.  
FOPT: Power off floating.

Notes:

1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Dummy source line follow LUTC for DSP/DRF
3. When SHD\_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition. It may have two condition: 0V or floating.
4. When RST\_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. Source/Gate/Border/VCOM will be released to floating

Restriction

**R01H (PWR): Power setting Register**

R01H	Bit											
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code	
PWR	W	0	0	0	0	0	0	0	0	1	01h	
1 <sup>st</sup> Parameter	W	1	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07h	
2 <sup>nd</sup> Parameter	W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h	
3 <sup>rd</sup> Parameter	W	1	-	VSPL_0 [6:0]								00h
4 <sup>th</sup> Parameter	W	1	-	VSP_1 [6:0]								00h
5 <sup>th</sup> Parameter	W	1	-	VSN_1 [6:0]								00h
6 <sup>th</sup> Parameter	W	1	-	VSPL_1 [6:0]								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	<p>-The command defines as :</p> <p>1<sup>st</sup> Parameter:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>VDG_EN</td> <td>Gate power selection. 0: External gate power from VGP/VGN 1: Internal DCDC function for generate VGP/VGN. (default)</td> </tr> <tr> <td>1</td> <td>VDS_EN</td> <td>Source power selection. 0: External source power from VSP/VSN pins. 1: Internal regulator function for generate VSP/VSN (default)</td> </tr> <tr> <td>2</td> <td>VSC_EN</td> <td>Source LV power selection. 0: External source power from VSPL pins. 1: Internal regulator function for generate VSPL (default)</td> </tr> </tbody> </table> <p>2<sup>nd</sup> Parameter:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1-0</td> <td>VGPN</td> <td>VGPN Voltage Level. 00: VGP=20 v, VGN=-20v. (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v</td> </tr> </tbody> </table>	Bit	Name	Description	0	VDG_EN	Gate power selection. 0: External gate power from VGP/VGN 1: Internal DCDC function for generate VGP/VGN. (default)	1	VDS_EN	Source power selection. 0: External source power from VSP/VSN pins. 1: Internal regulator function for generate VSP/VSN (default)	2	VSC_EN	Source LV power selection. 0: External source power from VSPL pins. 1: Internal regulator function for generate VSPL (default)	Bit	Name	Description	1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v. (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v
Bit	Name	Description																	
0	VDG_EN	Gate power selection. 0: External gate power from VGP/VGN 1: Internal DCDC function for generate VGP/VGN. (default)																	
1	VDS_EN	Source power selection. 0: External source power from VSP/VSN pins. 1: Internal regulator function for generate VSP/VSN (default)																	
2	VSC_EN	Source LV power selection. 0: External source power from VSPL pins. 1: Internal regulator function for generate VSPL (default)																	
Bit	Name	Description																	
1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v. (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v																	

3rd & 4th & 6th Parameter: Internal VSP\_1/VSPL\_0/ VSPL\_1 power selection

Bit	Name	Description								
6-0	VSP_1 & VSPL_0 & VSPL_1	Internal VSP & VSPL power selection.								
		bit[6:0]	Voltage(V)	bit [6:0]	Voltage(V)	bit [6:0]	Voltage(V)			
		0000000	00h	3	0101001	29h	7.1	1010010	52h	11.2
		0000001	01h	3.1	0101010	2Ah	7.2	1010011	53h	11.3
		0000010	02h	3.2	0101011	2Bh	7.3	1010100	54h	11.4
		0000011	03h	3.3	0101100	2Ch	7.4	1010101	55h	11.5
		0000100	04h	3.4	0101101	2Dh	7.5	1010110	56h	11.6
		0000101	05h	3.5	0101110	2Eh	7.6	1010111	57h	11.7
		0000110	06h	3.6	0101111	2Fh	7.7	1011000	58h	11.8
		0000111	07h	3.7	0110000	30h	7.8	1011001	59h	11.9
		0001000	08h	3.8	0110001	31h	7.9	1011010	5Ah	12
		0001001	09h	3.9	0110010	32h	8	1011011	5Bh	12.1
		0001010	0Ah	4	0110011	33h	8.1	1011100	5Ch	12.2
		0001011	0Bh	4.1	0110100	34h	8.2	1011101	5Dh	12.3
		0001100	0Ch	4.2	0110101	35h	8.3	1011110	5Eh	12.4
		0001101	0Dh	4.3	0110110	36h	8.4	1011111	5Fh	12.5
		0001110	0Eh	4.4	0110111	37h	8.5	1100000	60h	12.6
		0001111	0Fh	4.5	0111000	38h	8.6	1100001	61h	12.7
		0010000	10h	4.6	0111001	39h	8.7	1100010	62h	12.8
		0010001	11h	4.7	0111010	3Ah	8.8	1100011	63h	12.9
		0010010	12h	4.8	0111011	3Bh	8.9	1100100	64h	13
		0010011	13h	4.9	0111100	3Ch	9	1100101	65h	13.1
		0010100	14h	5	0111101	3Dh	9.1	1100110	66h	13.2
		0010101	15h	5.1	0111110	3Eh	9.2	1100111	67h	13.3
		0010110	16h	5.2	0111111	3Fh	9.3	1101000	68h	13.4
		0010111	17h	5.3	1000000	40h	9.4	1101001	69h	13.5
		0011000	18h	5.4	1000001	41h	9.5	1101010	6Ah	13.6
		0011001	19h	5.5	1000010	42h	9.6	1101011	6Bh	13.7
		0011010	1Ah	5.6	1000011	43h	9.7	1101100	6Ch	13.8
		0011011	1Bh	5.7	1000100	44h	9.8	1101101	6Dh	13.9
		0011100	1Ch	5.8	1000101	45h	9.9	1101110	6Eh	14
		0011101	1Dh	5.9	1000110	46h	10	1101111	6Fh	14.1
0011110	1Eh	6	1000111	47h	10.1	1110000	70h	14.2		
0011111	1Fh	6.1	1001000	48h	10.2	1110001	71h	14.3		
0100000	20h	6.2	1001001	49h	10.3	1110010	72h	14.4		
0100001	21h	6.3	1001010	4Ah	10.4	1110011	73h	14.5		
0100010	22h	6.4	1001011	4Bh	10.5	1110100	74h	14.6		
0100011	23h	6.5	1001100	4Ch	10.6	1110101	75h	14.7		
0100100	24h	6.6	1001101	4Dh	10.7	1110110	76h	14.8		
0100101	25h	6.7	1001110	4Eh	10.8	1110111	77h	14.9		
0100110	26h	6.8	1001111	4Fh	10.9	1111000	78h	15		
0100111	27h	6.9	1010000	50h	11	other	15			
0101000	28h	7	1010001	51h	11.1					

5th Parameter: Internal VSN\_1 power selection

Bit	Name	Description								
6-0	VSN_1	Internal VSN power selection.								
		bit[6:0]	Voltage(V)	bit [6:0]	Voltage(V)	bit [6:0]	Voltage(V)			
		0000000	00h	-3	0101001	29h	-7.1	1010010	52h	-11.2
		0000001	01h	-3.1	0101010	2Ah	-7.2	1010011	53h	-11.3
		0000010	02h	-3.2	0101011	2Bh	-7.3	1010100	54h	-11.4
		0000011	03h	-3.3	0101100	2Ch	-7.4	1010101	55h	-11.5
		0000100	04h	-3.4	0101101	2Dh	-7.5	1010110	56h	-11.6
		0000101	05h	-3.5	0101110	2Eh	-7.6	1010111	57h	-11.7
		0000110	06h	-3.6	0101111	2Fh	-7.7	1011000	58h	-11.8
		0000111	07h	-3.7	0110000	30h	-7.8	1011001	59h	-11.9
		0001000	08h	-3.8	0110001	31h	-7.9	1011010	5Ah	-12
		0001001	09h	-3.9	0110010	32h	-8	1011011	5Bh	-12.1
		0001010	0Ah	-4	0110011	33h	-8.1	1011100	5Ch	-12.2
		0001011	0Bh	-4.1	0110100	34h	-8.2	1011101	5Dh	-12.3
		0001100	0Ch	-4.2	0110101	35h	-8.3	1011110	5Eh	-12.4
		0001101	0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh	-12.5
		0001110	0Eh	-4.4	0110111	37h	-8.5	1100000	60h	-12.6
		0001111	0Fh	-4.5	0111000	38h	-8.6	1100001	61h	-12.7
		0010000	10h	-4.6	0111001	39h	-8.7	1100010	62h	-12.8
		0010001	11h	-4.7	0111010	3Ah	-8.8	1100011	63h	-12.9
		0010010	12h	-4.8	0111011	3Bh	-8.9	1100100	64h	-13
		0010011	13h	-4.9	0111100	3Ch	-9	1100101	65h	-13.1
		0010100	14h	-5	0111101	3Dh	-9.1	1100110	66h	-13.2
		0010101	15h	-5.1	0111110	3Eh	-9.2	1100111	67h	-13.3
		0010110	16h	-5.2	0111111	3Fh	-9.3	1101000	68h	-13.4
		0010111	17h	-5.3	1000000	40h	-9.4	1101001	69h	-13.5
		0011000	18h	-5.4	1000001	41h	-9.5	1101010	6Ah	-13.6
		0011001	19h	-5.5	1000010	42h	-9.6	1101011	6Bh	-13.7
		0011010	1Ah	-5.6	1000011	43h	-9.7	1101100	6Ch	-13.8
		0011011	1Bh	-5.7	1000100	44h	-9.8	1101101	6Dh	-13.9
		0011100	1Ch	-5.8	1000101	45h	-9.9	1101110	6Eh	-14
		0011101	1Dh	-5.9	1000110	46h	-10	1101111	6Fh	-14.1
		0011110	1Eh	-6	1000111	47h	-10.1	1110000	70h	-14.2
0011111	1Fh	-6.1	1001000	48h	-10.2	1110001	71h	-14.3		
0100000	20h	-6.2	1001001	49h	-10.3	1110010	72h	-14.4		
0100001	21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5		
0100010	22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6		
0100011	23h	-6.5	1001100	4Ch	-10.6	1110101	75h	-14.7		
0100100	24h	-6.6	1001101	4Dh	-10.7	1110110	76h	-14.8		
0100101	25h	-6.7	1001110	4Eh	-10.8	1110111	77h	-14.9		
0100110	26h	-6.8	1001111	4Fh	-10.9	1111000	78h	-15		
0100111	27h	-6.9	1010000	50h	-11	other	-15			
0101000	28h	-7	1010001	51h	-7.1					

Notes:

	<p>1. VSP_0/VSN_0 voltage output is <math>\pm 15</math> V fixed value.</p> <p>2. When switching Mode0 or Mode1, the voltage output is:                  Mode0: VSP_0(+15) / VSN_0 (-15) / VSPL_0 (+3~+15)                  Mode1: VSP_1(+3 ~ +15) / VSN_1(-3 ~ -15) / VSPL_1(+3 ~ +15)</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th></th> <th>Mode0</th> <th>Mode1</th> </tr> </thead> <tbody> <tr> <td>VSP</td> <td>VSP_0(+15)</td> <td>VSP_1(+3~+15)</td> </tr> <tr> <td>VSN</td> <td>VSN_0(-15)</td> <td>VSN_1(-3~-15)</td> </tr> <tr> <td>VSPL</td> <td>VSPL_0(+3~+15)</td> <td>VSPL_1(+3~+15)</td> </tr> </tbody> </table> <p>3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows                  I. VGP- VSP_0 / VSPL_0 / VSP_1 / VSPL_1 <math>\geq 2</math>v                  II. VGN- VSN_0 / VSN_1 <math>\geq -2</math>v                  For example:</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th></th> <th>symbol</th> <th>Voltage setting</th> <th>Real Voltage</th> </tr> </thead> <tbody> <tr> <td rowspan="10" style="vertical-align: middle;">Voltage</td> <td>VGP</td> <td>+10v</td> <td>+10v</td> </tr> <tr> <td>VGN</td> <td>-10v</td> <td>-10v</td> </tr> <tr> <td>VSP_0</td> <td>+15v</td> <td>+8v</td> </tr> <tr> <td>VSN_0</td> <td>-15v</td> <td>-8v</td> </tr> <tr> <td>VSP_1</td> <td>+5v</td> <td>+5v</td> </tr> <tr> <td>VSN_1</td> <td>-5v</td> <td>-5v</td> </tr> <tr> <td>VSPL</td> <td>+15v</td> <td>+8v</td> </tr> <tr> <td>VCOMH</td> <td>+15v+(-2v)</td> <td>+8v +(-2v)</td> </tr> <tr> <td>VCOML</td> <td>-15v+(-2v)</td> <td>-8v +(-2v)=-10 v</td> </tr> <tr> <td>VCOMDC</td> <td>-2v</td> <td>-2v</td> </tr> </tbody> </table>		Mode0	Mode1	VSP	VSP_0(+15)	VSP_1(+3~+15)	VSN	VSN_0(-15)	VSN_1(-3~-15)	VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)		symbol	Voltage setting	Real Voltage	Voltage	VGP	+10v	+10v	VGN	-10v	-10v	VSP_0	+15v	+8v	VSN_0	-15v	-8v	VSP_1	+5v	+5v	VSN_1	-5v	-5v	VSPL	+15v	+8v	VCOMH	+15v+(-2v)	+8v +(-2v)	VCOML	-15v+(-2v)	-8v +(-2v)=-10 v	VCOMDC	-2v	-2v
	Mode0	Mode1																																														
VSP	VSP_0(+15)	VSP_1(+3~+15)																																														
VSN	VSN_0(-15)	VSN_1(-3~-15)																																														
VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)																																														
	symbol	Voltage setting	Real Voltage																																													
Voltage	VGP	+10v	+10v																																													
	VGN	-10v	-10v																																													
	VSP_0	+15v	+8v																																													
	VSN_0	-15v	-8v																																													
	VSP_1	+5v	+5v																																													
	VSN_1	-5v	-5v																																													
	VSPL	+15v	+8v																																													
	VCOMH	+15v+(-2v)	+8v +(-2v)																																													
	VCOML	-15v+(-2v)	-8v +(-2v)=-10 v																																													
	VCOMDC	-2v	-2v																																													
Restriction																																																

**R02H (POF): Power OFF Command**

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H
1 <sup>st</sup> Parameter	W	0	-	-	-	-	-	-	-	-	00

NOTE: "-" Don't care, can be set to VDD or GND level

Description	<p>-The command defines as :</p> <p>R02h = 0x00h</p> <ul style="list-style-type: none"> <li>● After power off command, driver will power off base on power off sequence.</li> <li>● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N signal will rise from low to high.</li> <li>● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.</li> <li>● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.</li> </ul>
Restriction	This command only active when BUSY_N = "1".

**R04H (PON): Power ON Command**

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : <ul style="list-style-type: none"> <li>• After power on command, driver will power on base on power on sequence.</li> <li>• After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence (base on PWR command), BUSY_N signal will rise from low to high.</li> </ul>
Restriction	This command only active when BUSY_N = "1".

GOODDISPLAY

R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1 <sup>st</sup> Parameter	W	1	-	-	-	-	PHB_SFT [1:0]		PHA_SFT [1:0]		00h
2 <sup>nd</sup> Parameter	W	1	-	-	PHA_ON [5:0]						02h
3 <sup>rd</sup> Parameter	W	1	-	-	PHA_OFF [5:0]						07h
4 <sup>th</sup> Parameter	W	1	-	-	PHB_ON [5:0]						02h
5 <sup>th</sup> Parameter	W	1	-	-	PHB_OFF [5:0]						07h
6 <sup>th</sup> Parameter	W	1	-	-	PHC_ON [5:0]						02h
7 <sup>th</sup> Parameter	W	1	-	-	PHC_OFF [5:0]						07h

-The command define as follows:

1\*Parameter:

Bit	Name	Description
1-0	PHA_SFT	Soft start period of phase A: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS
3-2	PHB_SFT	Soft start period of phase B: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

Description

Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
000000	strength1	010110	strength23	101100	strength45
000001	strength2	010111	strength24	101101	strength46
000010	strength3	011000	strength25	101110	strength47
000011	strength4	011001	strength26	101111	strength48
000100	strength5	011010	strength27	110000	strength49
000101	strength6	011011	strength28	110001	strength50
000110	strength7	011100	strength29	110010	strength51
000111	strength8	011101	strength30	110011	strength52
001000	strength9	011110	strength31	110100	strength53
001001	strength10	011111	strength32	110101	strength54
001010	strength11	100000	strength33	110110	strength55
001011	strength12	100001	strength34	110111	strength56
001100	strength13	100010	strength35	111000	strength57
001101	strength14	100011	strength36	111001	strength58
001110	strength15	100100	strength37	111010	strength59
001111	strength16	100101	strength38	111011	strength60
010000	strength17	100110	strength39	111100	strength61
010001	strength18	100111	strength40	111101	strength62
010010	strength19	101000	strength41	111110	strength63
010011	strength20	101001	strength42	111111	strength64
010100	strength21	101010	strength43		
010101	strength22	101011	strength44		

Driving strength of PHA\_ON & PHB\_ON & PHC\_ON

Description	Minimum OFF time setting of PHA_OFF & PHB_OFF & PHC_OFF						
	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description	
	000000	Period1	010110	Period23	101100	Period45	
	000001	Period2	010111	Period24	101101	Period46	
	000010	Period3	011000	Period25	101110	Period47	
	000011	Period4	011001	Period26	101111	Period48	
	000100	Period5	011010	Period27	110000	Period49	
	000101	Period6	011011	Period28	110001	Period50	
	000110	Period7	011100	Period29	110010	Period51	
	000111	Period8	011101	Period30	110011	Period52	
	001000	Period9	011110	Period31	110100	Period53	
	001001	Period10	011111	Period32	110101	Period54	
	001010	Period11	100000	Period33	110110	Period55	
	001011	Period12	100001	Period34	110111	Period56	
	001100	Period13	100010	Period35	111000	Period57	
	001101	Period14	100011	Period36	111001	Period58	
	001110	Period15	100100	Period37	111010	Period59	
	001111	Period16	100101	Period38	111011	Period60	
	010000	Period17	100110	Period39	111100	Period61	
	010001	Period18	100111	Period40	111101	Period62	
	010010	Period19	101000	Period41	111110	Period63	
	010011	Period20	101001	Period42	111111	Period64	
	010100	Period21	101010	Period43			
	010101	Period22	101011	Period44			
Restriction							

**R07H (DSL P): Deep Sleep Command**

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSL P	W	0	0	0	0	0	0	1	1	1	07H
1 <sup>st</sup> Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

**R10H (DTM): Data Start transmission Register**

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM_master	W	0	0	0	0	1	0	0	0	0	10H
1 <sup>st</sup> Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h
⋮	W	1	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	00h
M <sup>th</sup> Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 12H. Then chip will start to send data/VCOM for panel.				
	Pixel [1~n][1:0]: 2-bit/pixel				
	Image Data	DDX=1(default)		DDX=0	
	Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
	00b	Gray0	ogray00	Gray3	ogray03
	01b	Gray1	ogray01	Gray2	ogray02
	10b	Gray2	ogray02	Gray1	ogray01
	11b	Gray3	ogray03	Gray0	ogray00
	Data mapping example: When DDX=1, Pixel[1:0]=01 -> Gray level select=Gray1, follow LUT data output from IP output port "ogray01".  When DDX=0, Pixel[1:0]=11 -> Gray level select=Gray0, follow LUT data output from IP output port "ogray00"				
Restriction					

**R11H (DSP): Data Stop Command**

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1 <sup>st</sup> Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as :				
	<ul style="list-style-type: none"> <li>While finished the data transmitting, user must send this command to driver and read Data_flag information.</li> </ul>				
	1*Parameter:				
	Bit	Name	Description		
	7	Data_flag	0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.		
	After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.				
Restriction	This command only actives when BUSY_N = "1".				

**R12H (DRF): Display Refresh Command**

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H
1 <sup>st</sup> Parameter	W	1	-	-	-	-	-	-	-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	<p>-The command defines as :</p> <p>R12H=0x00</p> <p>While users send this command, driver will refresh display base on SRAM data and LUT.</p> <p>After display refresh command, BUSY_N signal will become "0"</p>
Restriction	This command only actives when BUSY_N = "1"

**R17H (AUTO): Auto Sequence**

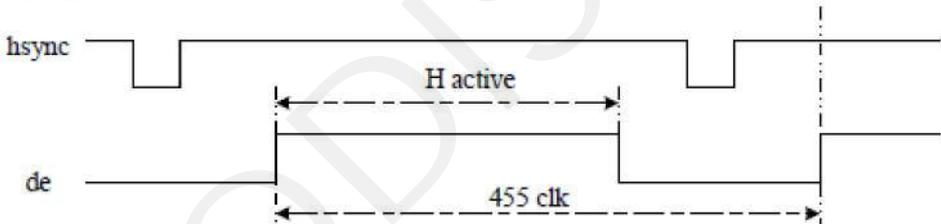
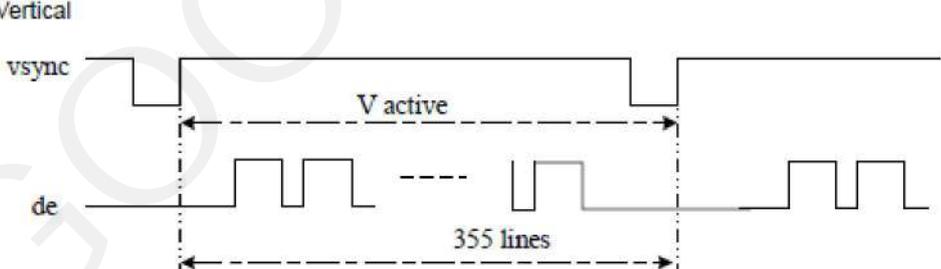
R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1 <sup>st</sup> Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	<p>The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.</p> <p>AUTO (0x17) + Code(0xA5) = (PON→DRF→POF)</p> <p>AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)</p>
Restriction	This command only actives when BUSY_N = "1".

R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1 <sup>st</sup> Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	02h

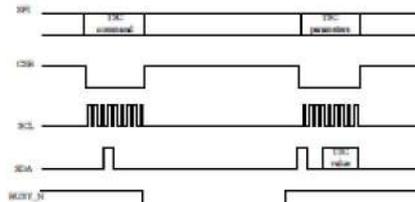
NOTE: "-" Don't care, can be set to VDD or GND level

Description	<p>-The command defines as:</p> <p>The command controls the PLL clock frequency. The PLL structure must support the following frame rates:</p> <table border="1" data-bbox="660 504 1019 622"> <thead> <tr> <th>bit3</th> <th>Dynamic frame rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable(default)</td> </tr> <tr> <td>1</td> <td>Enable</td> </tr> </tbody> </table> <table border="1" data-bbox="660 647 1019 987"> <thead> <tr> <th>FR[2:0]</th> <th>Frame rate</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>12.5 Hz</td> </tr> <tr> <td>001</td> <td>25 Hz</td> </tr> <tr> <td>010</td> <td>50 Hz(default)</td> </tr> <tr> <td>011</td> <td>65 Hz</td> </tr> <tr> <td>100</td> <td>75 Hz</td> </tr> <tr> <td>101</td> <td>85 Hz</td> </tr> <tr> <td>110</td> <td>100 Hz</td> </tr> <tr> <td>111</td> <td>120 Hz</td> </tr> </tbody> </table>	bit3	Dynamic frame rate	0	Disable(default)	1	Enable	FR[2:0]	Frame rate	000	12.5 Hz	001	25 Hz	010	50 Hz(default)	011	65 Hz	100	75 Hz	101	85 Hz	110	100 Hz	111	120 Hz
bit3	Dynamic frame rate																								
0	Disable(default)																								
1	Enable																								
FR[2:0]	Frame rate																								
000	12.5 Hz																								
001	25 Hz																								
010	50 Hz(default)																								
011	65 Hz																								
100	75 Hz																								
101	85 Hz																								
110	100 Hz																								
111	120 Hz																								
remark	<p>-Horizontal</p>  <p>-Vertical</p> 																								
Restriction																									

**R40H (TSC): Temperature Sensor Command**

R40H	Bit											
	Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	0	40H
1 <sup>st</sup> Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-	-
2 <sup>nd</sup> Parameter	R	1	D2/TS[9]	D1/TS[8]	D0	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	<p>-The command define as follows:                  This command indicates the temperature value.                  If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.                  If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value</p> 																																																																																																																																																																										
	<table border="1"> <thead> <tr> <th>TS[7:0]/D[10:3]</th> <th>T (°C)</th> <th>TS[7:0]/D[10:3]</th> <th>T (°C)</th> <th>TS[7:0]/D[10:3]</th> <th>T (°C)</th> </tr> </thead> <tbody> <tr><td>11100111</td><td>-25</td><td>00000000</td><td>0</td><td>00011001</td><td>25</td></tr> <tr><td>11101000</td><td>-24</td><td>00000001</td><td>1</td><td>00011010</td><td>26</td></tr> <tr><td>11101001</td><td>-23</td><td>00000010</td><td>2</td><td>00011011</td><td>27</td></tr> <tr><td>11101010</td><td>-22</td><td>00000011</td><td>3</td><td>00011100</td><td>28</td></tr> <tr><td>11101011</td><td>-21</td><td>00000100</td><td>4</td><td>00011101</td><td>29</td></tr> <tr><td>11101100</td><td>-20</td><td>00000101</td><td>5</td><td>00011110</td><td>30</td></tr> <tr><td>11101101</td><td>-19</td><td>00000110</td><td>6</td><td>00011111</td><td>31</td></tr> <tr><td>11101110</td><td>-18</td><td>00000111</td><td>7</td><td>00100000</td><td>32</td></tr> <tr><td>11101111</td><td>-17</td><td>00001000</td><td>8</td><td>00100001</td><td>33</td></tr> <tr><td>11110000</td><td>-16</td><td>00001001</td><td>9</td><td>00100010</td><td>34</td></tr> <tr><td>11110001</td><td>-15</td><td>00001010</td><td>10</td><td>00100011</td><td>35</td></tr> <tr><td>11110010</td><td>-14</td><td>00001011</td><td>11</td><td>00100100</td><td>36</td></tr> <tr><td>11110011</td><td>-13</td><td>00001100</td><td>12</td><td>00100101</td><td>37</td></tr> <tr><td>11110100</td><td>-12</td><td>00001101</td><td>13</td><td>00100110</td><td>38</td></tr> <tr><td>11110101</td><td>-11</td><td>00001110</td><td>14</td><td>00100111</td><td>39</td></tr> <tr><td>11110110</td><td>-10</td><td>00001111</td><td>15</td><td>00101000</td><td>40</td></tr> <tr><td>11110111</td><td>-9</td><td>00010000</td><td>16</td><td>00101001</td><td>41</td></tr> <tr><td>11111000</td><td>-8</td><td>00010001</td><td>17</td><td>00101010</td><td>42</td></tr> <tr><td>11111001</td><td>-7</td><td>00010010</td><td>18</td><td>00101011</td><td>43</td></tr> <tr><td>11111010</td><td>-6</td><td>00010011</td><td>19</td><td>00101100</td><td>44</td></tr> <tr><td>11111011</td><td>-5</td><td>00010100</td><td>20</td><td>00101101</td><td>45</td></tr> <tr><td>11111100</td><td>-4</td><td>00010101</td><td>21</td><td>00101110</td><td>46</td></tr> <tr><td>11111101</td><td>-3</td><td>00010110</td><td>22</td><td>00101111</td><td>47</td></tr> <tr><td>11111110</td><td>-2</td><td>00010111</td><td>23</td><td>00110000</td><td>48</td></tr> <tr><td>11111111</td><td>-1</td><td>00011000</td><td>24</td><td>00110001</td><td>49</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>TS[9:8]</th> <th>T (°C)</th> </tr> </thead> <tbody> <tr><td>00</td><td>+0</td></tr> <tr><td>01</td><td>+0.25</td></tr> <tr><td>10</td><td>+0.5</td></tr> <tr><td>11</td><td>+0.75</td></tr> </tbody> </table>						TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	11100111	-25	00000000	0	00011001	25	11101000	-24	00000001	1	00011010	26	11101001	-23	00000010	2	00011011	27	11101010	-22	00000011	3	00011100	28	11101011	-21	00000100	4	00011101	29	11101100	-20	00000101	5	00011110	30	11101101	-19	00000110	6	00011111	31	11101110	-18	00000111	7	00100000	32	11101111	-17	00001000	8	00100001	33	11110000	-16	00001001	9	00100010	34	11110001	-15	00001010	10	00100011	35	11110010	-14	00001011	11	00100100	36	11110011	-13	00001100	12	00100101	37	11110100	-12	00001101	13	00100110	38	11110101	-11	00001110	14	00100111	39	11110110	-10	00001111	15	00101000	40	11110111	-9	00010000	16	00101001	41	11111000	-8	00010001	17	00101010	42	11111001	-7	00010010	18	00101011	43	11111010	-6	00010011	19	00101100	44	11111011	-5	00010100	20	00101101	45	11111100	-4	00010101	21	00101110	46	11111101	-3	00010110	22	00101111	47	11111110	-2	00010111	23	00110000	48	11111111	-1	00011000	24	00110001	49	TS[9:8]	T (°C)	00	+0	01	+0.25	10	+0.5	11
TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)																																																																																																																																																																						
11100111	-25	00000000	0	00011001	25																																																																																																																																																																						
11101000	-24	00000001	1	00011010	26																																																																																																																																																																						
11101001	-23	00000010	2	00011011	27																																																																																																																																																																						
11101010	-22	00000011	3	00011100	28																																																																																																																																																																						
11101011	-21	00000100	4	00011101	29																																																																																																																																																																						
11101100	-20	00000101	5	00011110	30																																																																																																																																																																						
11101101	-19	00000110	6	00011111	31																																																																																																																																																																						
11101110	-18	00000111	7	00100000	32																																																																																																																																																																						
11101111	-17	00001000	8	00100001	33																																																																																																																																																																						
11110000	-16	00001001	9	00100010	34																																																																																																																																																																						
11110001	-15	00001010	10	00100011	35																																																																																																																																																																						
11110010	-14	00001011	11	00100100	36																																																																																																																																																																						
11110011	-13	00001100	12	00100101	37																																																																																																																																																																						
11110100	-12	00001101	13	00100110	38																																																																																																																																																																						
11110101	-11	00001110	14	00100111	39																																																																																																																																																																						
11110110	-10	00001111	15	00101000	40																																																																																																																																																																						
11110111	-9	00010000	16	00101001	41																																																																																																																																																																						
11111000	-8	00010001	17	00101010	42																																																																																																																																																																						
11111001	-7	00010010	18	00101011	43																																																																																																																																																																						
11111010	-6	00010011	19	00101100	44																																																																																																																																																																						
11111011	-5	00010100	20	00101101	45																																																																																																																																																																						
11111100	-4	00010101	21	00101110	46																																																																																																																																																																						
11111101	-3	00010110	22	00101111	47																																																																																																																																																																						
11111110	-2	00010111	23	00110000	48																																																																																																																																																																						
11111111	-1	00011000	24	00110001	49																																																																																																																																																																						
TS[9:8]	T (°C)																																																																																																																																																																										
00	+0																																																																																																																																																																										
01	+0.25																																																																																																																																																																										
10	+0.5																																																																																																																																																																										
11	+0.75																																																																																																																																																																										
Restriction	This command only actives when BUSY_N = "1".																																																																																																																																																																										

**R41H (TSE): Temperature Sensor Calibration Register**

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1 <sup>st</sup> Parameter	W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the driver IC temperature sensor enable and calibration function.	
	Reserve one temperature offset TO[3:0] for calibration 1. TO[3]: mean '+' or '-', while 0 is '+' ; 1 is '-' 2. TO[2:0]: mean temperature offset value	
	Bit	Name
	Description	
3-0	TO[3:0]	Temperature level: 0000: +0°C (default) 0001: +0.5°C 0010: +1°C 0011: +1.5°C 0100: +2°C 0101: +2.5°C 0110: +3°C 0111: +3.5°C 1000: -4°C 1001: -3.5°C 1010: -3°C 1011: -2.5°C 1100: -2°C 1101: -1.5°C 1110: -1°C 1111: -0.5°C
4	TO[4]	0: +0.0°C (default) 1: +0.25°C
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.
Restriction	This command only actives after R04H(PON)	

**R42H (TSW): Temperature Sensor Write Register**

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1 <sup>st</sup> Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2 <sup>nd</sup> Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3 <sup>rd</sup> Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as:	
	This command writes the temperature.	
	1 <sup>st</sup> Parameter:	
	Bit	Name Description
	2-0	WATTR[2:0] Pointer setting
	5-3	WATTR[5:3] User-defined address bits (A2, A1, A0)
	7-6	WATTR[7:6] I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1 <sup>st</sup> parameter) 11: 4 bytes (head byte + pointer + 1 <sup>st</sup> parameter + 2 <sup>nd</sup> parameter)
	2 <sup>nd</sup> Parameter:	
	Bit	Name Description
	7-0	WMSB[7:0] MSByte of write-data to external temperature sensor
3 <sup>rd</sup> Parameter:		
Bit	Name Description	
7-0	WLSB[7:0] LSByte of write-data to external temperature sensor	
Restriction	This command only actives after R04H(PON)	

**R43H (TSR): Temperature Sensor Read Register**

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSR	W	0	0	1	0	0	0	0	1	1	43H
1 <sup>st</sup> Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2 <sup>nd</sup> Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as:  This command reads the temperature sensed by the temperature sensor. 1 <sup>st</sup> Parameter:											
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7-0</td> <td>RMSB[7:0]</td> <td>MSByte of read-data from external temperature sensor</td> </tr> </tbody> </table> 2 <sup>nd</sup> Parameter: <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7-0</td> <td>RLSB[7:0]</td> <td>LSByte of write-data from external temperature sensor</td> </tr> </tbody> </table>	Bit	Name	Description	7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor	Bit	Name	Description	7-0	RLSB[7:0]
Bit	Name	Description										
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor										
Bit	Name	Description										
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor										
Restriction	This command only actives after R04H(PON)											

R50H (CDI): VCOM and DATA interval setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1 <sup>st</sup> Parameter	W	1	VBD[2]	VBD[1]	VBD [0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

NOTE: "-" Don't care, can be set to VDD or GND level

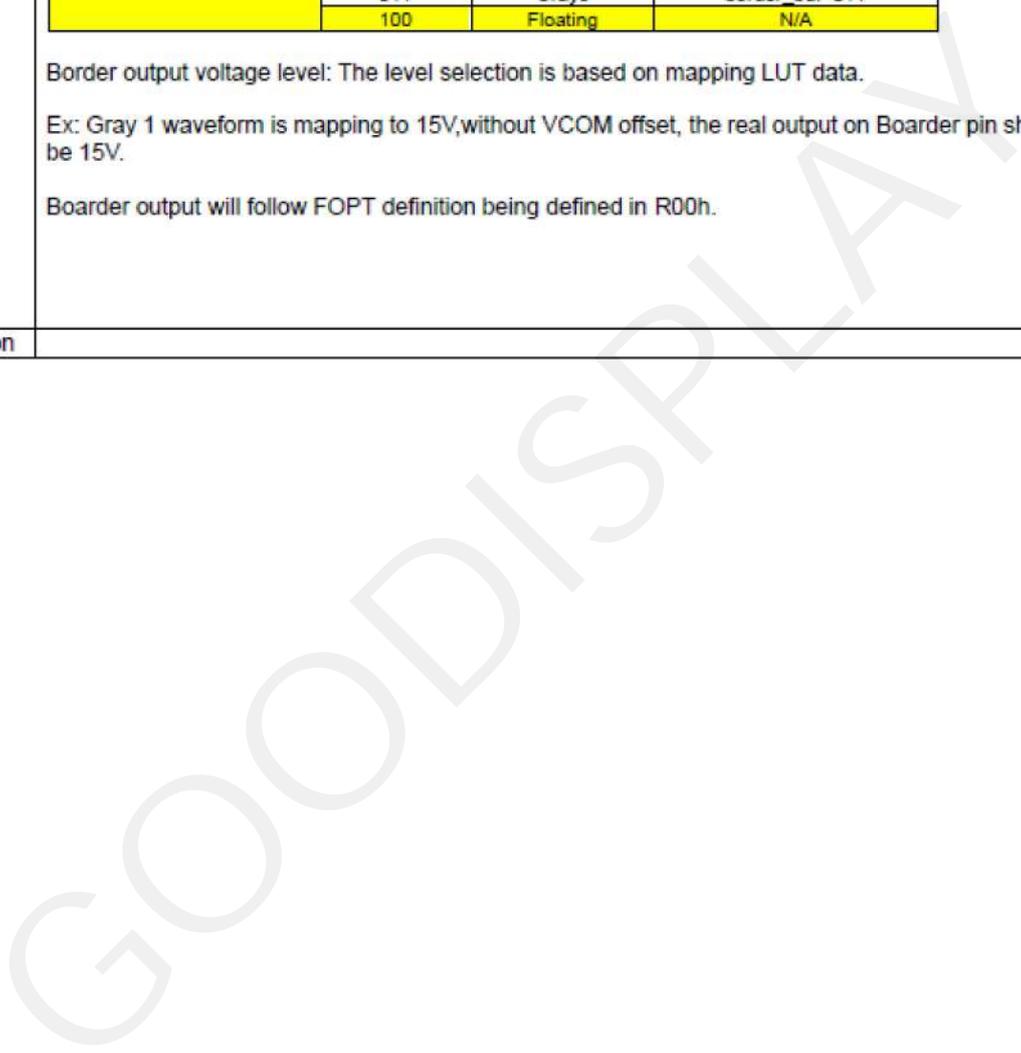
**Description**

-The command defines as:  
 This command can set 2 kinds of parameters, 1.VCOM to data output interval(CDI)  
 :  
 CDI[3:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (55hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync(default) 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync

The diagram shows the timing of VCOM and data output. Key signals include Internal vsync, Internal hsync, Internal de, VCOM, and Source data Output. A red arrow labeled 'CDI setting' indicates the interval between the start of VCOM output and the start of source data output. A dashed line marks the '55 hsync-CDI setting (fixed)' point.

	VBD[2:0]: Border data selection. (from LUT output by IP port border_w[1:0])			
	This register will make boarder pin output being mapped to a certain gray scale.			
	<b>Bit 4</b>	<b>Bit7-5</b>	<b>Description</b>	
	DDX	VBD[2:0]	Gray level	
	0	000	Floating	N/A
		001	Gray3	border_buf=011
		010	Gray2	border_buf=010
		011	Gray1	border_buf=001
		100	Gray0	border_buf=000
	1 (default)	000	Gray0	border_buf=000
001		Gray1	border_buf=001	
010		Gray2	border_buf=010	
011		Gray3	border_buf=011	
	100	Floating	N/A	
Border output voltage level: The level selection is based on mapping LUT data.				
Ex: Gray 1 waveform is mapping to 15V,without VCOM offset, the real output on Boarder pin shall be 15V.				
Boarder output will follow FOPT definition being defined in R00h.				
Restriction				



**R51H (LPD): Lower Power Detection Register**

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1 <sup>st</sup> Parameter	R	1	-	-	-	-	-	-	-	LPD	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	<p>-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD&lt;2.5v, which could be select in RE4H (LVSEL)).</p> <p>1<sup>st</sup> Parameter:</p> <table border="1"> <tr> <td>Bit 0</td> <td>LPD</td> </tr> <tr> <td>0</td> <td>Low power input.</td> </tr> <tr> <td>1</td> <td>Normal status.</td> </tr> </table>	Bit 0	LPD	0	Low power input.	1	Normal status.
Bit 0	LPD						
0	Low power input.						
1	Normal status.						
Restriction	This command only actives when BUSY_N = "1".						

**R61H (TRES): Resolution setting**

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1 <sup>st</sup> Parameter	W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
2 <sup>nd</sup> Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
3 <sup>th</sup> Parameter	W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
4 <sup>th</sup> Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	<p>-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES</p> <p><b>Note:</b> No matter HRES[9],HRES[1:0],VRES[9] value being filled, it's always be 00b.</p> <p>Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[9:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:2]*4-1</p> <p style="text-align: center;">EX :400X300 GD: First G active = G0 LAST active GD= 0+300-1= 299; (G299) SD : First active channel: =S0 LAST active SD=0+100*4-1=399; (S399)</p>
Restriction	Horizontal resolution should be 4-multiple.

**R65H (GSST): Gate/Source Start Setting Register**

R65H	Bit										
Inst/Para	RW	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1 <sup>st</sup> Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2 <sup>nd</sup> Parameter	W	1	S_start[7]	S_start[8]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h
3 <sup>rd</sup> Parameter	W	1	-	-	-	gscan	-	-	G_start[9]	G_start[8]	00h
4 <sup>th</sup> Parameter	W	1	G_start[7]	G_start[8]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

-The command define as follows:

**Note:**  
 No matter S\_start[9], S\_start [1:0], G\_start[9] value being filled, it's always be 00b.

- S\_Start [8:0] describe which source output line is the first date line
- G\_Start[8:0] describe which gate line is the first scan line
- gscan :Gate scan select  
 0: Normal scan(default)  
 1: Cascade type scan

Scanning mode setting ( gscan=1): 800x300

Resolution: 300x300

Source lines: S0, S1, S198, S199

Gate lines: G0, G1, G148, G149, G150, G151, G298, G299

Gold Bumps JD79668 MS=1 (left) and MS=0 (right)

Restriction: S\_Start should be the multiple of 4

**R70H (REV): REVISION register**

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1 <sup>st</sup> Parameter	R	1	0	0	0	0	0	0	1	1	06h
2 <sup>nd</sup> Parameter	R	1	0	0	0	0	0	0	1	0	02h
3 <sup>rd</sup> Parameter	R	1	0	0	0	0	0	0	0	1	01h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as:	
	1 <sup>st</sup> & 2 <sup>nd</sup> & 3 <sup>rd</sup> Parameter:	
	Bit	Description
	7-0	CHIP_REV
Restriction		

R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1 <sup>st</sup> Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the IC status. Host can read this data to understand the IC status.										
	1 <sup>st</sup> Parameter:										
	Bit	Name	Description								
	0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable								
	1	AMV	AMV: Analog signal 0: Get Vcom value from R81h(default) 1: Get Vcom value in analog signal								
	2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSPL_0 during Auto Measure VCOM period.								
	3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.								
	5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 5s (default) 01: 10s 10: 15s 11: 20s								
	7-6	P[1:0]	The sensing points of sampling time 00: 2 (default) 01: 4 10: 8 11: 16 Sampling time = the last quarter of sensing time (T) VCOM = average of N points. N=2,4,8,16								
	<p>The diagram shows three signals: Source voltage (constant high), Vcom (constant high), and BUSY_N (pulsed low). A red horizontal line indicates the 'Status of Vcom controlled by sensing mode' during the BUSY_N pulse. A double-headed arrow shows 'The last quarter of sensing time' at the end of the BUSY_N pulse. Below the BUSY_N signal, it is noted that the Vcom is the 'Average of N point. N=2,4,8,16'.</p>										
Restriction	This command only actives when BUSY_N = "1".										

R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	RW	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1 <sup>st</sup> Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command could get the VCOM value											
	1 <sup>st</sup> Parameter:											
6-0	VV[6:0]	VCOM value										
		VV [6:0]	Voltage(V)	VV [6:0]	Voltage(V)	VV [6:0]	Voltage(V)	VV [6:0]	Voltage(V)	VV [6:0]	Voltage(V)	
		0000000	00h	0	0011100	1Ch	-1.4	0111000	38h	-2.8		
		0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85		
		0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9		
		0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95		
		0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3		
		0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05		
		0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1		
		0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15		
		0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2		
		0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25		
		0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3		
		0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35		
		0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4		
		0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45		
		0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5		
		0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55		
		0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6		
		0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65		
		0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7		
		0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75		
		0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8		
		0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85		
		0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9		
		0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95		
		0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4		
0011001	19h	-1.25	0110101	35h	-2.65	other		-4				
0011010	1Ah	-1.3	0110110	36h	-2.7							
0011011	1Bh	-1.35	0110111	37h	-2.75							
Restriction												

**R82H (VDCS): VCOM\_DC Setting Register**

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1 <sup>st</sup> Parameter	W	1	-	VDCS[6]	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command set the VCOM DC value. Driver will base on this value for VCM_DC. 1 <sup>st</sup> Parameter:																		
	Bit	Name	Description																
6-0	VDCS[6:0]	<b>VCOM value</b>																	
		VDCS [6:0]	Voltage(V)	VDCS [6:0]	Voltage(V)	VDCS [6:0]	Voltage(V)	VDCS [6:0]	Voltage(V)	VDCS [6:0]	Voltage(V)								
		0000000	00h	0(default)	0011100	1Ch	-1.4	0111000	38h	-2.8	0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
		0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9	0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
		0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3	0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
		0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1	0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
		0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2	0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
		0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3	0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
		0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4	0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
		0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5	0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
		0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6	0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
		0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7	0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
		0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8	0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
		0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9	0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
		0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4	0011001	19h	-1.25	0110101	35h	-2.65	other		-4
		0011010	1Ah	-1.3	0110110	36h	-2.7				0011011	1Bh	-1.35	0110111	37h	-2.75			

Restriction

**R83H (PTL): Partial Window Register**

R83H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1 <sup>st</sup> Parameter	W	1	-	-	-	PTH_ENB	-	-	HRST[9]	HRST[8]	00h
2 <sup>nd</sup> Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	-	-	00h
3 <sup>rd</sup> Parameter	W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4 <sup>th</sup> Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	-	-	00h
5 <sup>th</sup> Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
6 <sup>th</sup> Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
7 <sup>th</sup> Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
8 <sup>th</sup> Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
9 <sup>th</sup> Parameter	W	1	-	-	-	-	-	-	-	PMODE	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-This command sets partial window.														
	<table border="1"> <thead> <tr> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>HRST[9:2]</td> <td>Horizontal start address</td> </tr> <tr> <td>HRED[9:2]</td> <td>Horizontal end address. HRED must be greater than HRST.</td> </tr> <tr> <td>VRST[9:0]</td> <td>Vertical start address.</td> </tr> <tr> <td>VRED[9:0]</td> <td>Vertical end address. VRED must be greater than VRST.</td> </tr> <tr> <td>PMODE</td> <td>0: disable partial mode(default) 1: enable partial mode</td> </tr> <tr> <td>PTH_ENB</td> <td>0:Source output enable follow HRST and HRED 1:Source output disable</td> </tr> </tbody> </table> <p>Note: No matter HRST[1:0] ,HRST[9],HRED[9],VRST[9],VRED[9] value being filled, it's always be 00b. No matter HRED[1:0] value being filled, it's always be 11b.</p> <p>Gates scan both inside and outside of the partial window.</p>	Name	Description	HRST[9:2]	Horizontal start address	HRED[9:2]	Horizontal end address. HRED must be greater than HRST.	VRST[9:0]	Vertical start address.	VRED[9:0]	Vertical end address. VRED must be greater than VRST.	PMODE	0: disable partial mode(default) 1: enable partial mode	PTH_ENB	0:Source output enable follow HRST and HRED 1:Source output disable
Name	Description														
HRST[9:2]	Horizontal start address														
HRED[9:2]	Horizontal end address. HRED must be greater than HRST.														
VRST[9:0]	Vertical start address.														
VRED[9:0]	Vertical end address. VRED must be greater than VRST.														
PMODE	0: disable partial mode(default) 1: enable partial mode														
PTH_ENB	0:Source output enable follow HRST and HRED 1:Source output disable														
Restriction															

**R90H (PGM): Program Mode**

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	0	1	0	0	0	0	90H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	

**R91H (APG): Active Program**

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

GOODDISPLAY

R92H (RMTP): Read MTP Data

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMTP	W	0	1	0	0	1	0	0	1	0	92H
1 <sup>st</sup> Parameter	R	1	Dummy								-
2 <sup>nd</sup> Parameter	R	1	The data of address 0x000 in the MTP								-
3 <sup>rd</sup> Parameter	R	1	The data of address 0x001 in the MTP								-
4 <sup>th</sup> Parameter	R	1	:								-
5 <sup>th</sup> Parameter	R	1	The data of address (n-1) in the MTP								-
6 <sup>th</sup> ~(m-1) <sup>th</sup> Parameter	R	1	.....								-
m <sup>th</sup> Parameter	R	1	The data of address (n) in the MTP								-

NOTE: "-" Don't care, can be set to VDD or GND level

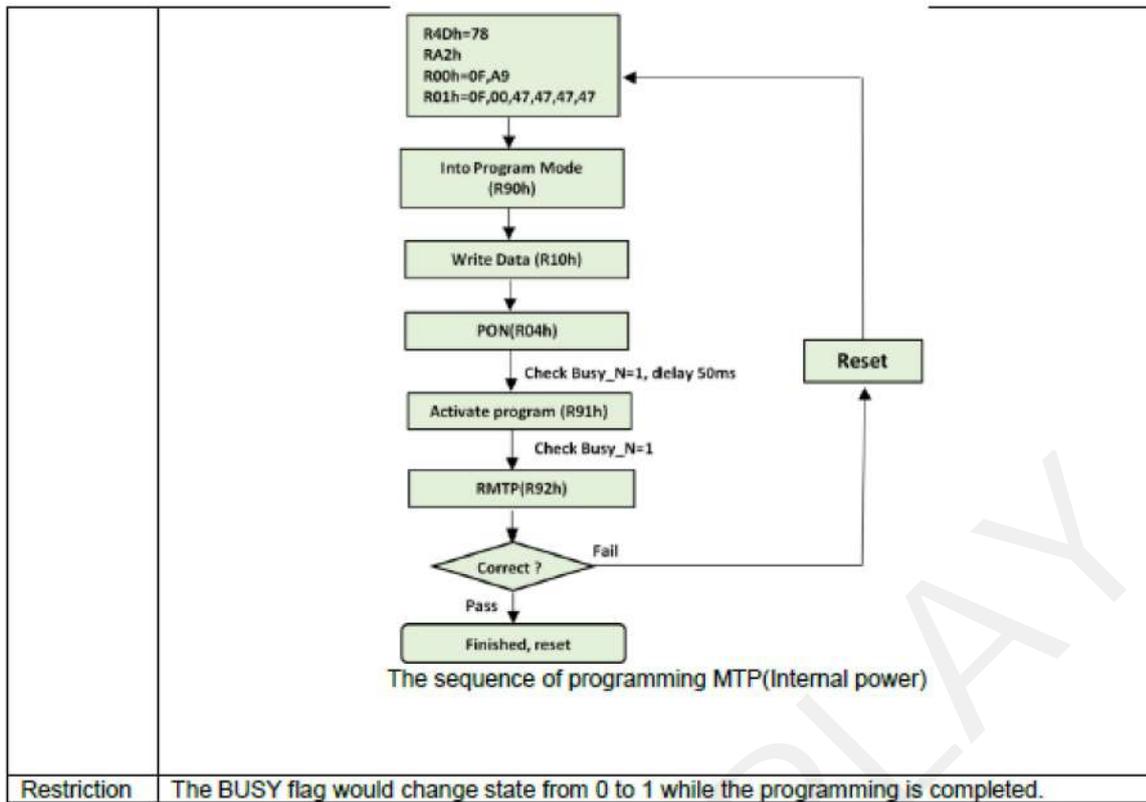
Description

The command define as follows:  
 -The command is used for reading the content of MTP for checking the data of programming,  
 -The value of (n) is depending on the amount of programmed data, the max address= 0xFF

```

    graph TD
      RA2h[RA2h] --> R90h[Into Program Mode R90h]
      R90h --> R10h[Write Data R10h]
      R10h -- "Apply VMTP=10.1v" --> R91h[Activate program R91h]
      R91h -- "Check Busy_N=1, then remove VMTP" --> R92h[RMTP R92h]
      R92h --> Correct{Correct?}
      Correct -- Fail --> Reset[Reset]
      Reset --> RA2h
      Correct -- Pass --> Finished[Finished, reset]
    
```

The sequence of programming MTP(External power)

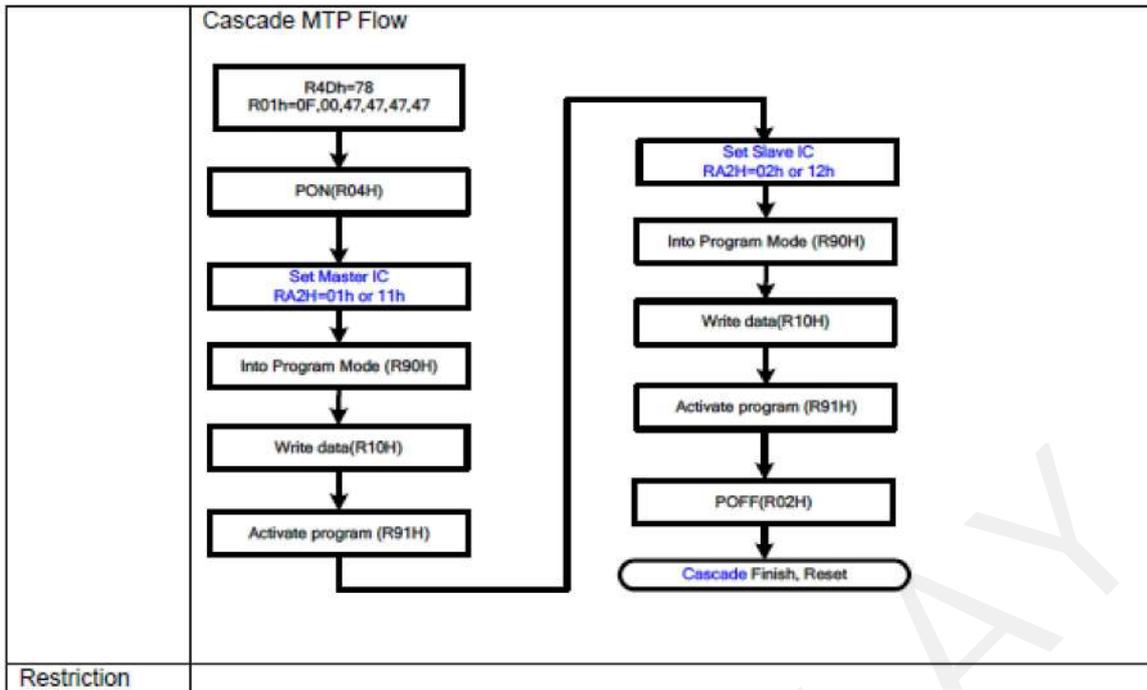


**RA2 (PGM\_CFG): MTP Program Config Register**

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM_CFG	W	0	1	0	1	0	0	0	1	0	A2H
1 <sup>st</sup> Parameter	W	1	-	-	-	VMTPSEL	-	-	M_dis	S_dis	00h
2 <sup>nd</sup> Parameter	W	1	PGM_SADDR[15:8]								00h
3 <sup>rd</sup> Parameter	W	1	PGM_SADDR[7:0]								00h
4 <sup>th</sup> Parameter	W	1	PGM_DSIZE[15:8]								0Fh
5 <sup>th</sup> Parameter	W	1	PGM_DSIZE[7:0]								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for setting configuration of MTP		
	1 <sup>st</sup> Parameter:		
	Bit	Name	Description
	0	S_dis	0: slave enable some command (default) 1: slave disable some command
	1	M_dis	0: master enable some command (default) 1: master disable some command
	4	VMTPSEL	0: External VMTP (default) 1: Internal VMTP
	Bit[0] enable/disable some command when IC sets slave (MS pin is low)		
	Bit[1] enable/disable some command when IC sets master (MS pin is high)		
	Note: Some command define: R00H(Parameter 1) (PSR), R10H(DTM), R90H(PGM), R91H(APG), R83H(PTLW)		
	Command read		
M_dis	S_dis	Description	
0	0	command read from master	
0	1	command read from master	
1	0	command read from slave	
1	1	command read from slave	
2 <sup>nd</sup> & 3 <sup>rd</sup> Parameters: Program and Read MTP start address PGM_SADDR[15:0]			
4 <sup>th</sup> & 5 <sup>th</sup> Parameters: Program data size PGM_DSIZE[15:0]			
Note: If user program Area0 (0x00~0x017F), PGM_SADDR[15:0] will be set 0x0000, PGM_DSIZE[15:0] will be set 0x0180.			



**RE0H (CCSET): Cascade Setting**

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1 <sup>st</sup> Parameter	W	1	-	-	-	-	-	-	-	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade.	
	1 <sup>st</sup> Parameter:	
	Bit	Description
	0	CCEIN Output clock enable/disable. 0: Output 0V at SyncC pin. (default) 1: Output clock at SyncC pin for slave chip.
Restriction		

**RE3H (PWS): Power Saving Register**

RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1 <sup>st</sup> Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h

NOTE: "-" Don't care, can be set to VDD or GND level

- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM\_W: VCOM power saving width (unit = line period)

SD\_W: Source power saving width (unit = 500nS),  $SD\_W \leq S2G$

Description

Restriction

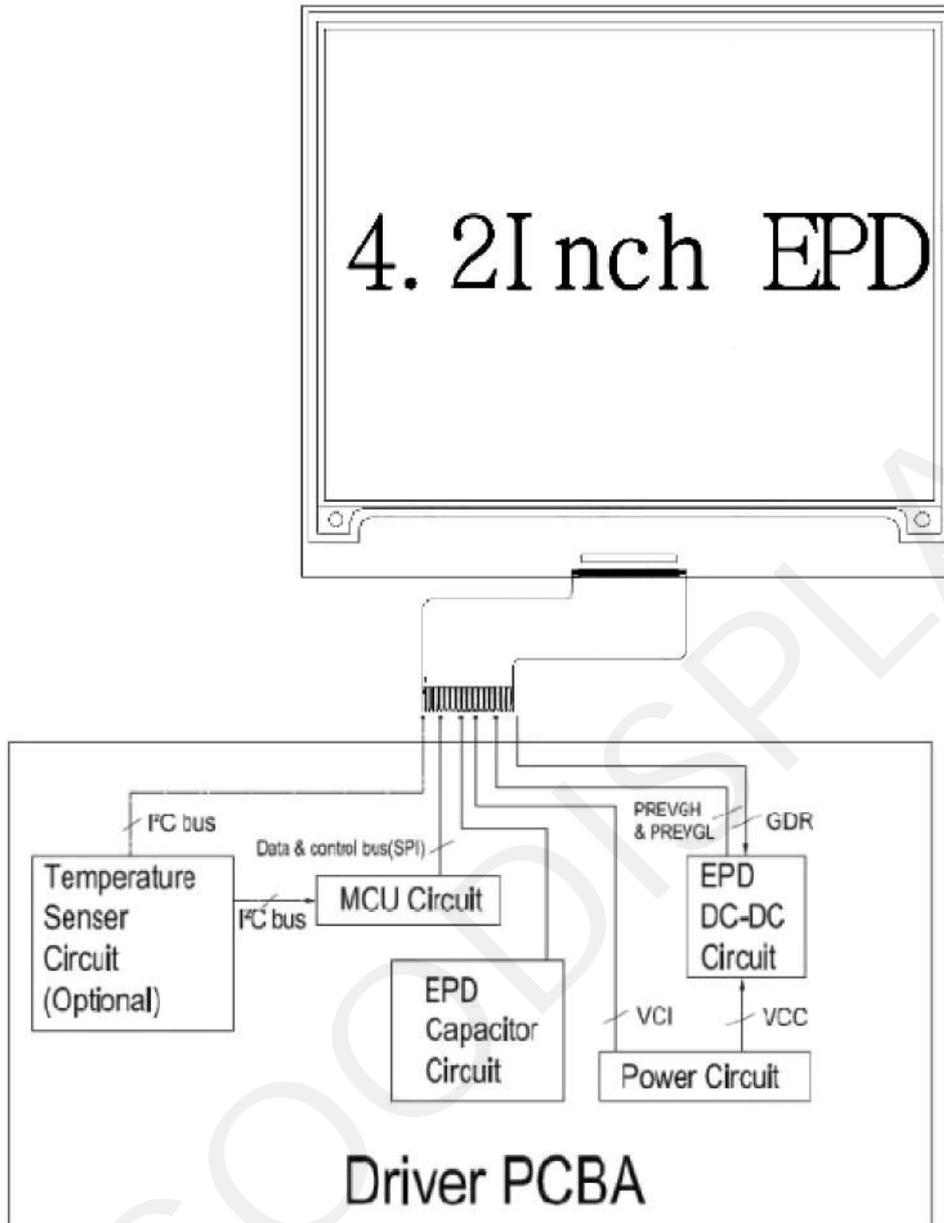
**RE4H (LVSEL): LVD Voltage Select Register**

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1 <sup>st</sup> Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

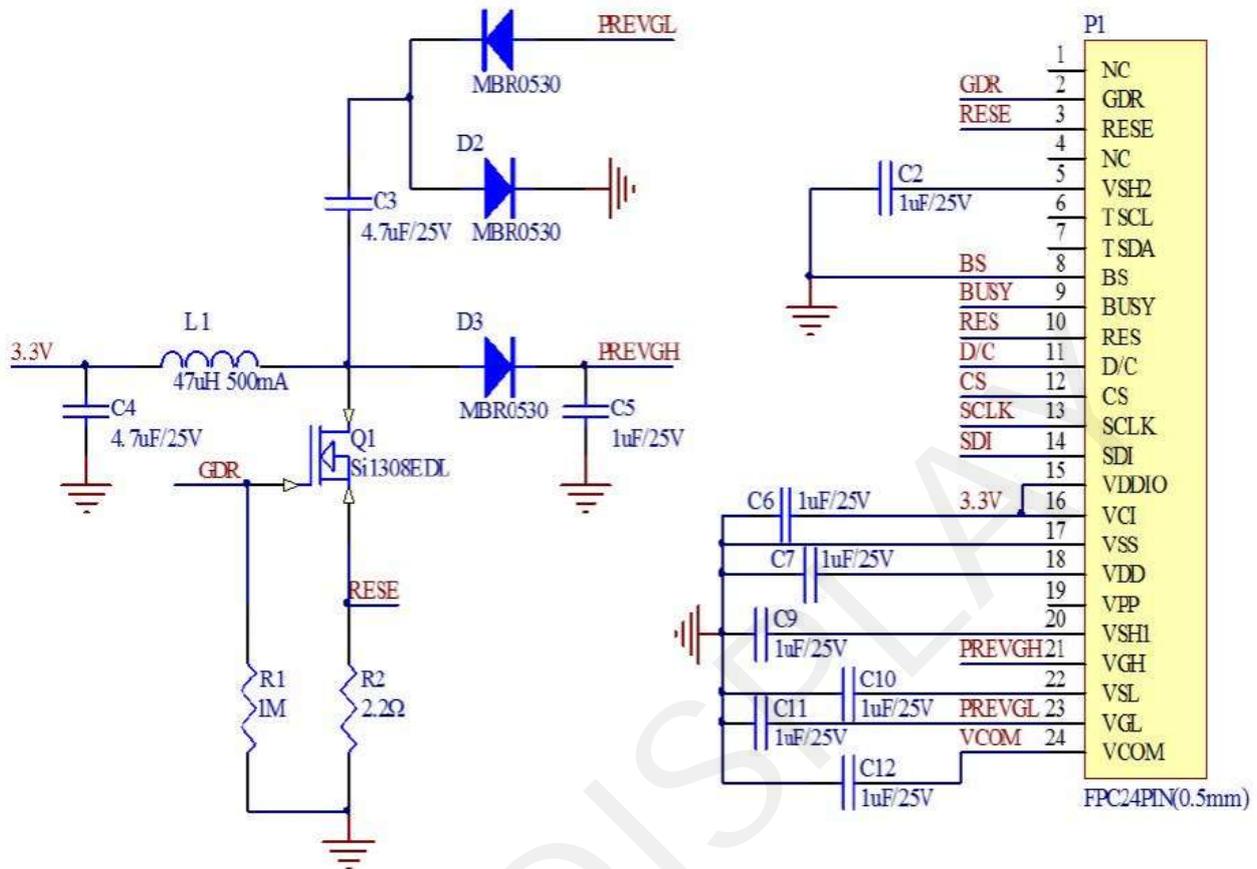
NOTE: "-" Don't care, can be set to VDD or GND level

Description	LVD_SEL[1:0]: Low Power Voltage Selection	
	LVD_SEL[1:0]	LVD value
	00	< 2.2 V
	01	< 2.3 V
	10	< 2.4 V
	11	< 2.5 V (default)
Restriction		

### 8. Block Diagram



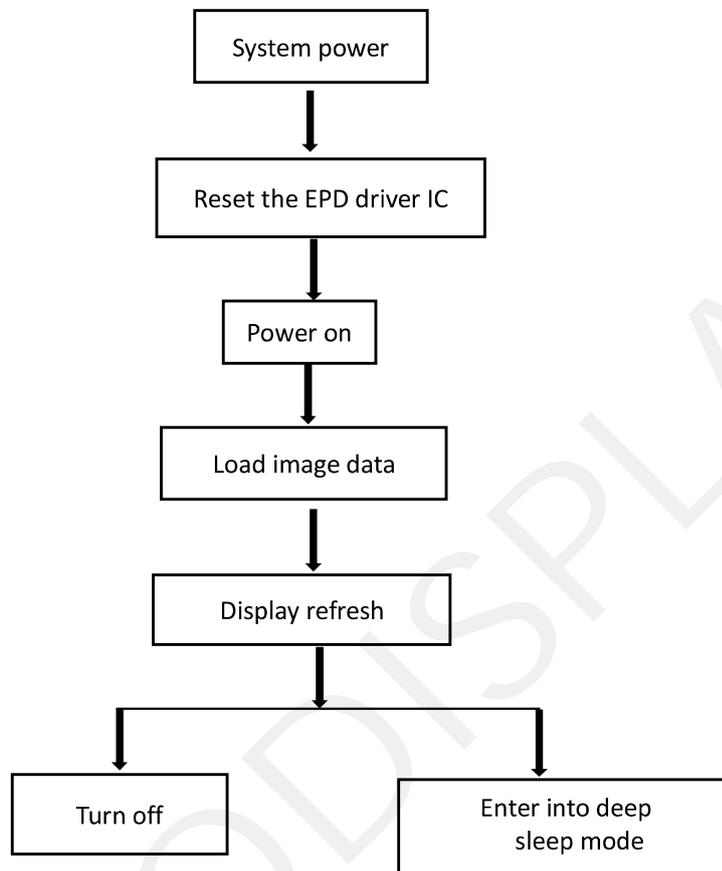
## 9. Typical Application Circuit with SPI Interface



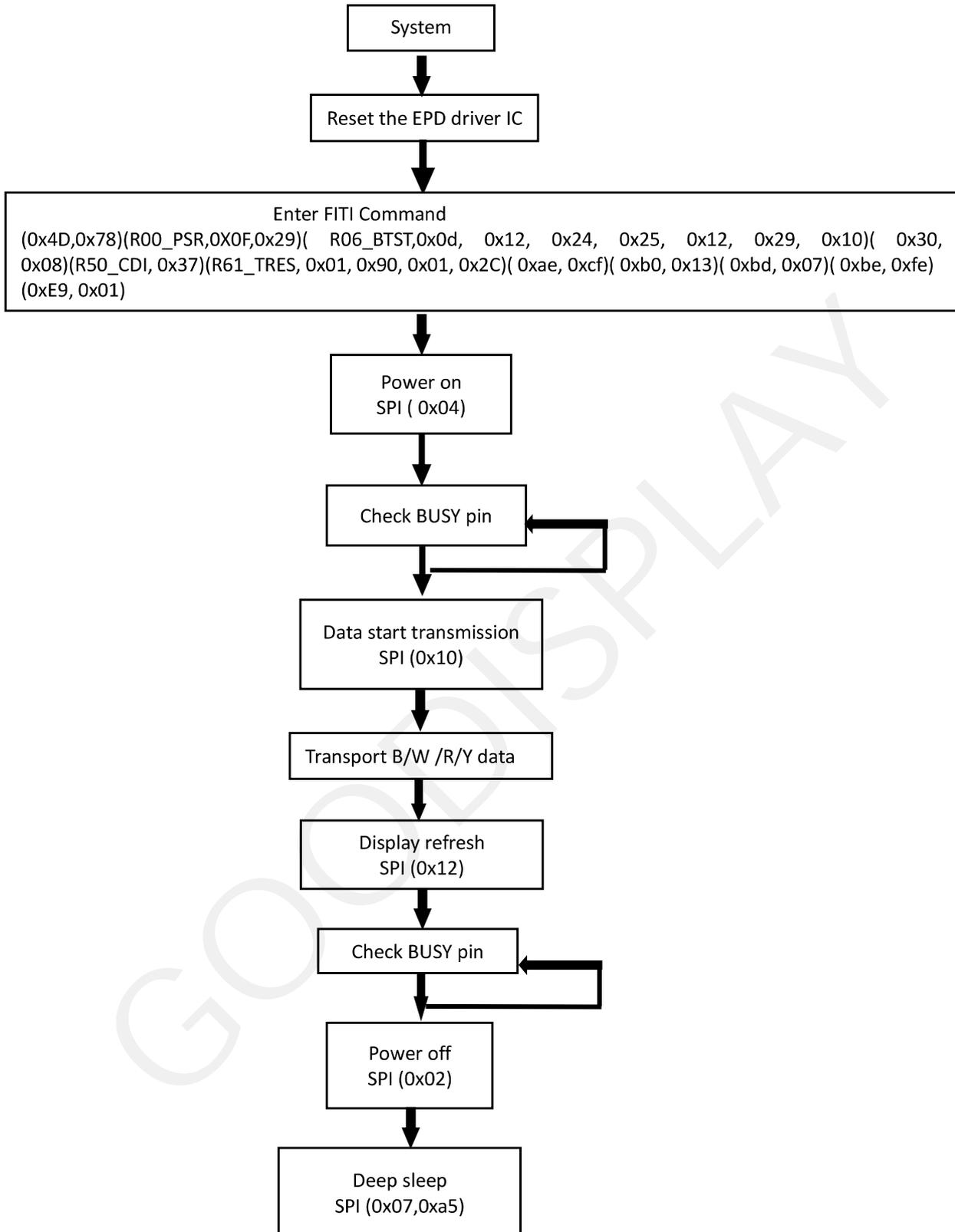
Part Name	Requirements for spare part
C1—C12	0603/0805; X5R/X7R; Voltage Rating: $\geq 25V$
R1、R2	0603/0805; 1% variation, $\geq 0.05W$
D1—D3	MBR0530: 1) Reverse DC Voltage $\geq 30V$ 2) $I_o \geq 500mA$ 3) Forward voltage $\leq 430mV$
Q1	Si1308EDL: 1) Drain-Source breakdown voltage $\geq 30V$ 2) $V_{gs(th)} \leq 1.5V$ 3) $R_{ds(on)} \leq 400m\Omega$
L1	refer to NR3015: $I_o = 500mA(max)$
P1	24pins, 0.5mm pitch

## 10. Typical Operating Sequence

### 10.1 LUT from OTP Operation Flow



## 10.2 OTP Operation Reference Program Code



## 11. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 500 h Test in white pattern
2	High-Temperature Storage	T=60°C, RH=35%, 500h Test in white pattern
3	High-Temperature Operation	T=40°C, RH=30%, 500h
4	Low-Temperature Operation	0°C, 500h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=90%, 500h
6	High- Temperature, High -Humidity Storage	T=60°C, RH=80%, 500h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 100 cycles Test in white pattern

**Note: 1. Stay white pattern for storage and non-operation test.**

**2. Operation is black→white→red→yellow pattern, the interval is 150s.**

**3. Put in 20°C--25°C for 1hour after test finished, The function ,appearance and display performance is OK.**

## 12. Quality Assurance

### 12.1 Environment

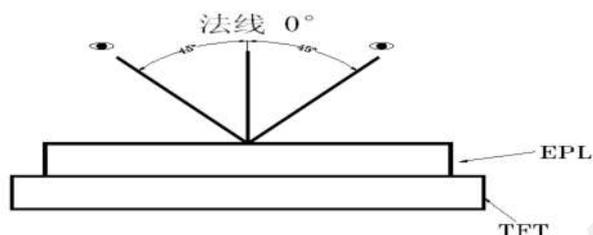
Temperature: 18~28°C

Humidity: 40%~70%RH

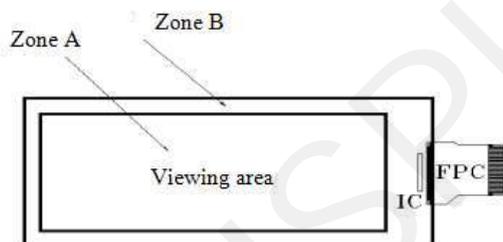
### 12.2 Illuminance

Brightness: 800~1500LUX; Angle: Relate  $45 \pm 5^\circ$  surround; Function check when 150 ~ 200 LUX visual distance module surface 30CM

### 12.3 Inspect method



### 12.4 Display are



### 12.5 Ghosting test method

Four-color ghosting is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by Good Display



1) Measurement Instruments: X-rite i1Pro

2) Ghosting formula:

W ghosting:  $\Delta E = \text{Max} (\Delta E_{ab}(Y-W, R-W), \Delta E_{ab}(Y-W, W-W), \Delta E_{ab}(Y-W, B-W), \Delta E_{ab}(R-W, W-W), \Delta E_{ab}(R-W, B-W), \Delta E_{ab}(W-W, B-W))$

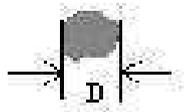
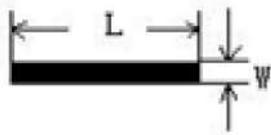
K ghosting:  $\Delta E = \text{Max} (\Delta E_{ab}(Y-B, R-B), \Delta E_{ab}(Y-B, W-B), \Delta E_{ab}(Y-B, B-B), \Delta E_{ab}(R-B, W-B), \Delta E_{ab}(R-B, B-B), \Delta E_{ab}(W-B, B-B))$

R ghosting:  $\Delta E = \text{Max} (\Delta E_{ab}(Y-R, R-R), \Delta E_{ab}(Y-R, W-R), \Delta E_{ab}(Y-R, B-R), \Delta E_{ab}(R-R, W-R), \Delta E_{ab}(R-R, B-R), \Delta E_{ab}(W-R, B-R))$

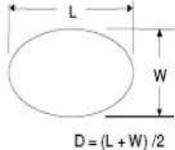
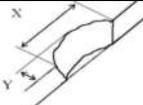
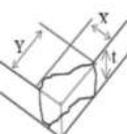
Y ghosting:  $\Delta E = \text{Max} (\Delta E_{ab}(Y-Y, R-Y), \Delta E_{ab}(Y-Y, W-Y), \Delta E_{ab}(Y-Y, B-Y), \Delta E_{ab}(R-Y, W-Y), \Delta E_{ab}(R-Y, B-Y), \Delta E_{ab}(W-Y, B-Y))$

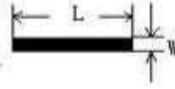
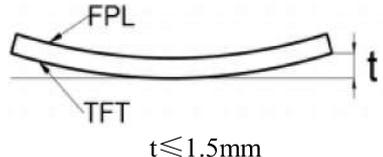
## 12.6 Inspection standard

### 12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA		
2	Black/White spots	 $D \leq 0.3\text{mm}$ , Allowed $0.3\text{mm} < D \leq 0.5\text{mm}$ . $N \leq 5$ allowable $D > 0.5\text{mm}$ is not allowed	MI	Visual inspection	Zone A
3	Black/White lines (No switch)	 $L \leq 1.0\text{mm}$ , $W \leq 0.15\text{mm}$ negligible $1.0\text{mm} < L \leq 4.0\text{mm}$ $0.15\text{mm} < W \leq 0.5\text{mm}$ $N \leq 4$ allowable $L > 4.0\text{mm}$ , $W > 0.5\text{mm}$ is not allowed		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A

**12.6.2 Appearance inspection standard**

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 <p><math>D \leq 0.3\text{mm}</math>, Allowed  <math>0.3\text{mm} &lt; D \leq 0.5\text{mm}</math>, <math>N \leq 5</math>  <math>D &gt; 0.5\text{mm}</math>, Not Allow</p>	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 <p><math>X \leq 3\text{mm}</math>, <math>Y \leq 0.5\text{mm}</math> And without affecting the electrode is permissible</p>  <p><math>2\text{mm} \leq X</math> or <math>2\text{mm} \leq Y</math> t= not counted.and without affecting the electrode , permissible</p>  <p><math>W \leq 0.1\text{mm}</math>, <math>L \leq 5\text{mm}</math>, without affecting the electrode , <math>n \leq 2</math></p>	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 <p>Not Allow</p>	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  <p>Not Allow</p>	MA	Visual / Microscope	Zone B

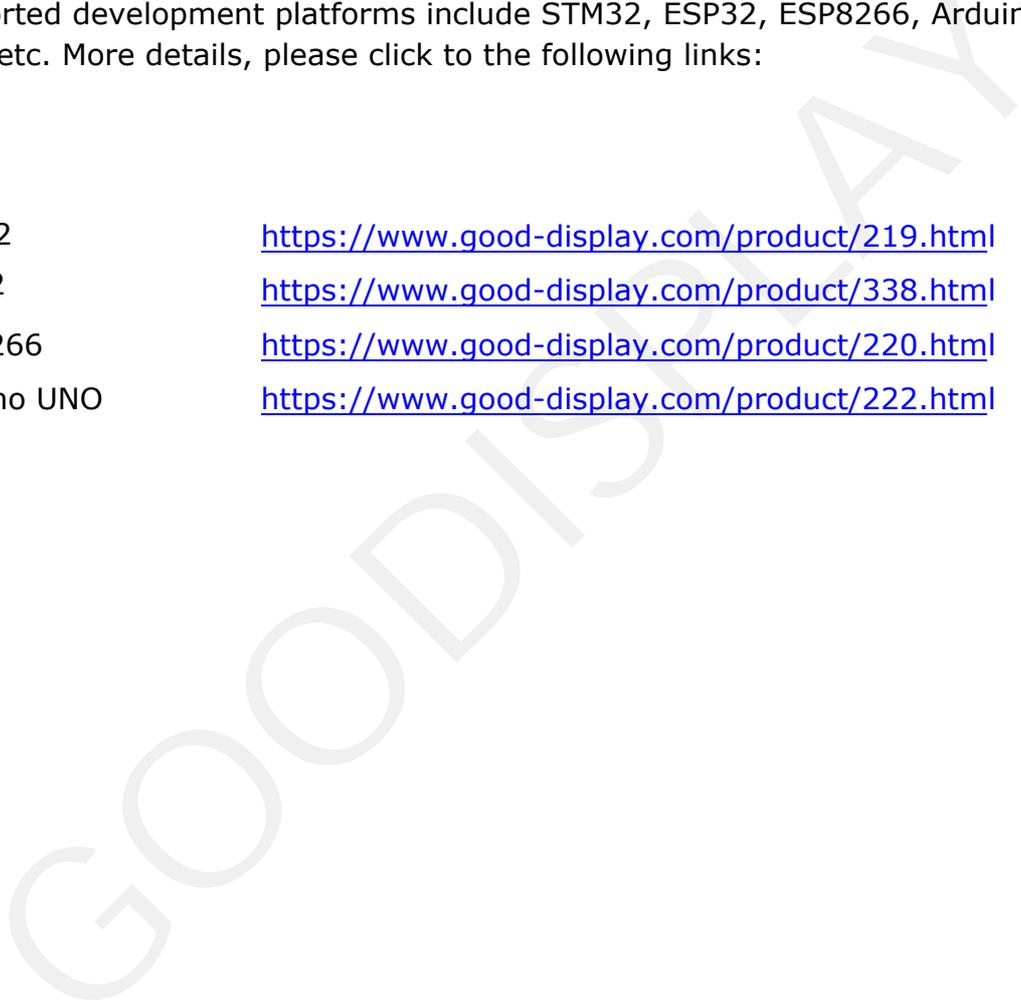
8	B/W Line	 <p> <math>L \leq 1.0\text{mm}, W \leq 0.15\text{mm}</math> negligible  <math>1.0\text{mm} &lt; L \leq 4.0\text{mm}</math>  <math>0.15\text{mm} &lt; W \leq 0.5\text{mm}</math>  <math>N \leq 4</math> allowable  <math>L &gt; 4.0\text{mm}, W &gt; 0.5\text{mm}</math> is not allowed                 </p>	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	TFT edge bulge: $X \leq 3\text{mm}, Y \leq 0.3\text{mm}$ Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	$D \leq 0.25\text{mm}$ , allow $0.25\text{mm} < D \leq 0.4\text{mm}, n \leq 4$ allow $D > 0.4\text{mm}$ is not allowed ( $n \leq 8$ items are allowed within 5 mm in diameter)	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl $\leq 1\%$	MI		
12	Edge glue height/ Edge glue bubble	Edge Adhesives $H \leq$ PS surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width Length excluding Edge adhesives bubble: bubble Width $\leq 1/2$ Margin width; Length $\leq 5.0\text{mm}$ . $n \leq 5$	MI	Visual / Ruler	Zone B
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	
14	Silicon glue	Thickness $\leq$ PS surface(With protect film): Full cover the IC; Shape: The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 <p> <math>t \leq 1.5\text{mm}</math> </p>	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

### 13. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color (black, white, red and yellow) Good Display 's E-paper Display. And it is also added the functions of USB serial port, FLASH chip, font chip, current detection ect.

Development Kit consists of the development board and the pinboard. Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc. More details, please click to the following links:

STM32	<a href="https://www.good-display.com/product/219.html">https://www.good-display.com/product/219.html</a>
ESP32	<a href="https://www.good-display.com/product/338.html">https://www.good-display.com/product/338.html</a>
ESP8266	<a href="https://www.good-display.com/product/220.html">https://www.good-display.com/product/220.html</a>
Arduino UNO	<a href="https://www.good-display.com/product/222.html">https://www.good-display.com/product/222.html</a>



## 14. Handling, Safety and Environmental Requirements

<b>WARNING</b>
<p>The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.</p>

<b>CAUTION</b>
<p>The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.</p>
<p>Disassembling the display module can cause permanent damage and invalidate the warranty agreements.</p>

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

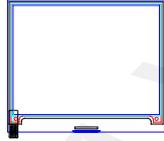
<b>Data sheet status</b>	
Product specification	The data sheet contains final product specifications.
<b>Limiting values</b>	
<p>Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device.</p> <p>These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.</p>	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

<b>Product Environmental certification</b>
RoHS

### 15. Packaging

## PACKING INSTRUCTION

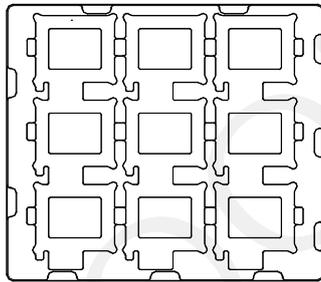
P/N	Customer Code	Ref. P/N	Type	PKG Method	Marking	Surface Marks	Pull Tape
			GLASS	Blister	BACK	None	YES

Packing Materials List					9PCS/LAYER, 20LAYER/CTN, TOTAL 180PCS/CTN.
List	Model	Materials	Q'ty	Unit	Pull tape: 
Carton	7# 417*362*229 mm	corrugate	1	Piece	
Inner Carton	7#(INNER)400*343 *95 mm	corrugate	2	Piece	
Blister		PET	22	Piece	
Thin foam	295.6*269.6*T1.8~2.0mm	EPE	20	Piece	
Antistatic vacuum bag	450*590*0.075		2	Piece	
Foam board		EPE	5	Piece	
PULL TAPE	16*5*T0.05		180	Piece	

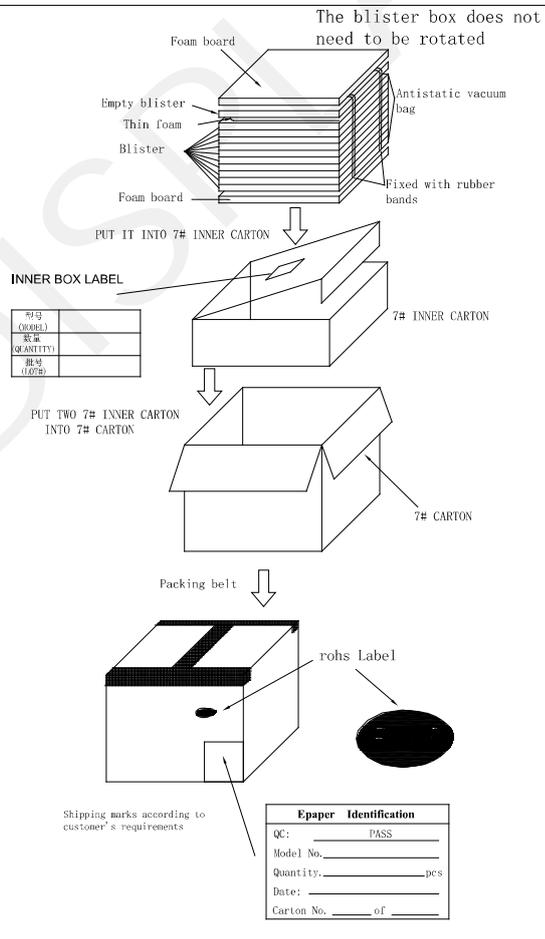
Detail:

Blister box:

Note: there are 20 layers of products, divided into 2 inner boxes, and an empty blister box is placed on the top of each inner box, so the number of blister boxes is 22



QUANTITY: 9PCS



## 16. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.
- (7) For more precautions, please click on the link:  
<https://www.good-display.com/news/80.html>