JADARD

JD79676AA

Data Sheet

All-in-one driver with
TCON for Color application

Version 1.0.4
2023/07/06

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1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 2-bit output per pixel. The timing controller provides control signals for the source driver and gate drivers.

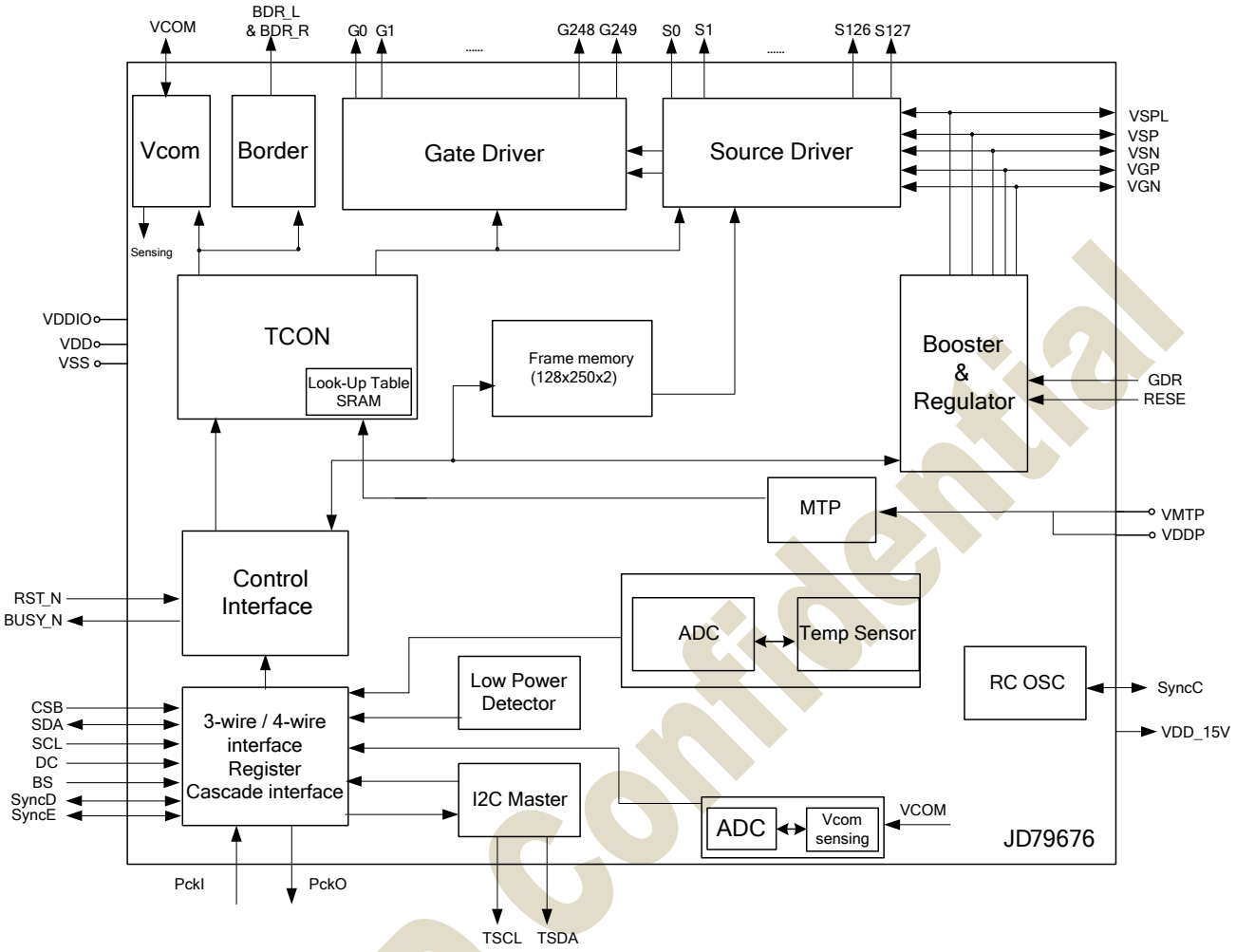
The DC-DC controller allows to generate the source output voltage VSP_0/VSN_0(+/-15V),VSP_1/VSPL_0/VSPL_1/VSN_1 (+/-3V~+/-15V) and VGP/VGN(+/-20V, +/-17V, +/-15V, +/-10V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire(SPI) serial.

2. FEATURES

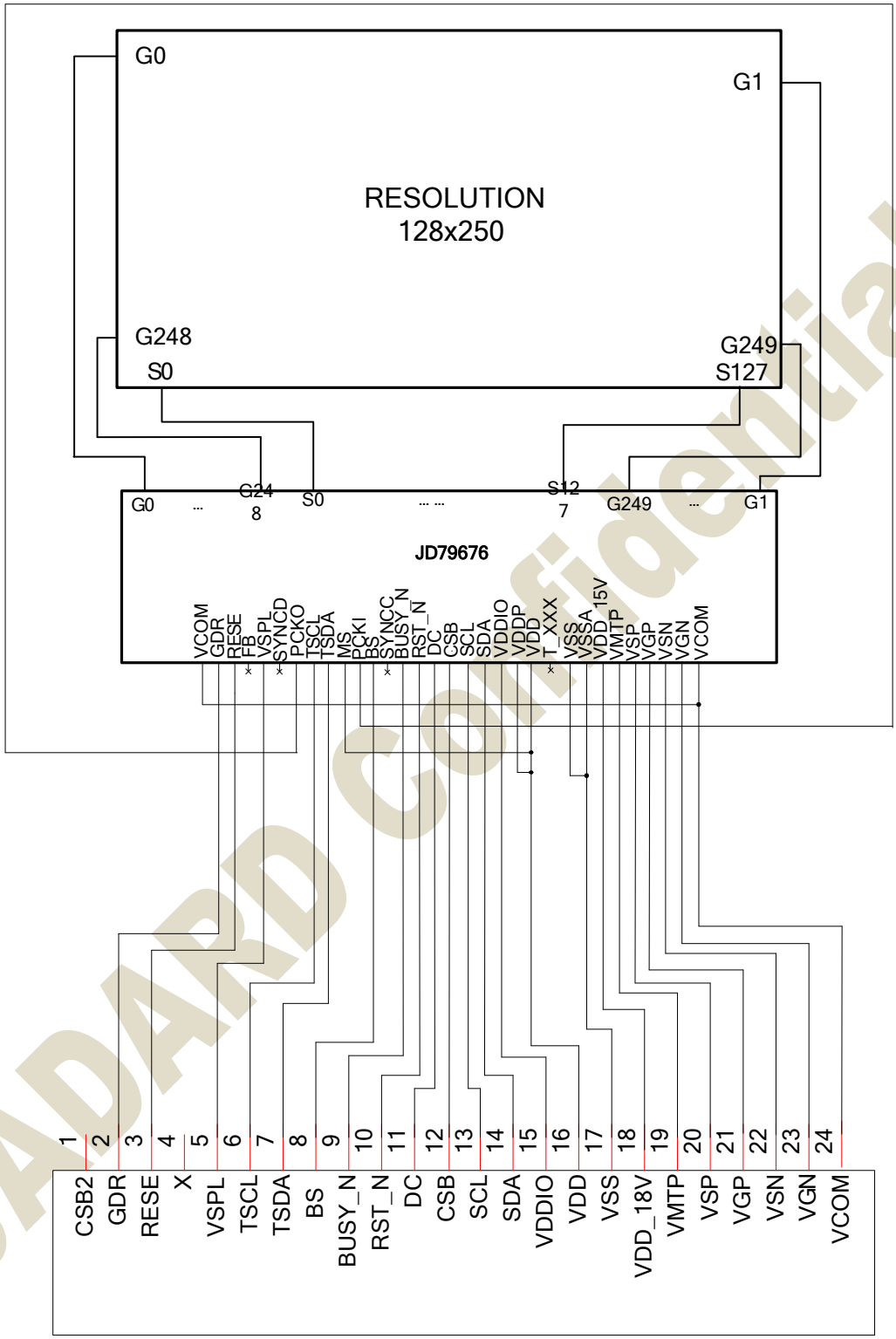
- System-on-chip (SOC) for color application
- Timing controller support several all resolution (maximum resolution 128x250)
- Support source & gate driver function:
  - 128 Outputs source driver with 2-bit black/white/red/yellow per pixel:
    - Output dynamic range(Voltage step:100mV):
      - Mode 0: 0V & VSP_0(+15V) & VSN_0(-15V) & VSPL_0(+3V~+15V)
      - Mode 1: 0V & VSP_1 (+3V ~ +15V) & VSN_1(-3V ~ -15V) & VSPL_1 (+3V ~ +15V)
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame)
    - Left and Right shift capability
  - 250 Output gate driver:
    - Output dynamic range: VGP and VGN(+/-20V, +/-17V, +/-15V, +/-10V)
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (7-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: 128 x 250 x 2 bit SRAM
- Built in temperature sensor:
  - On-Chip: -25 ^{o}C ~50 ^{o}C ± 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}< 2.2V~2.5V)
- PLL : On-chip RC oscillator
- 3-wire/4-wire (SPI) serial interface for system configuration
- Digital supply voltage: 2.3~3.6V
- 4.0 K-byte MTP for LUT, User command
- Partial update

- Support cascade
- Package-COG

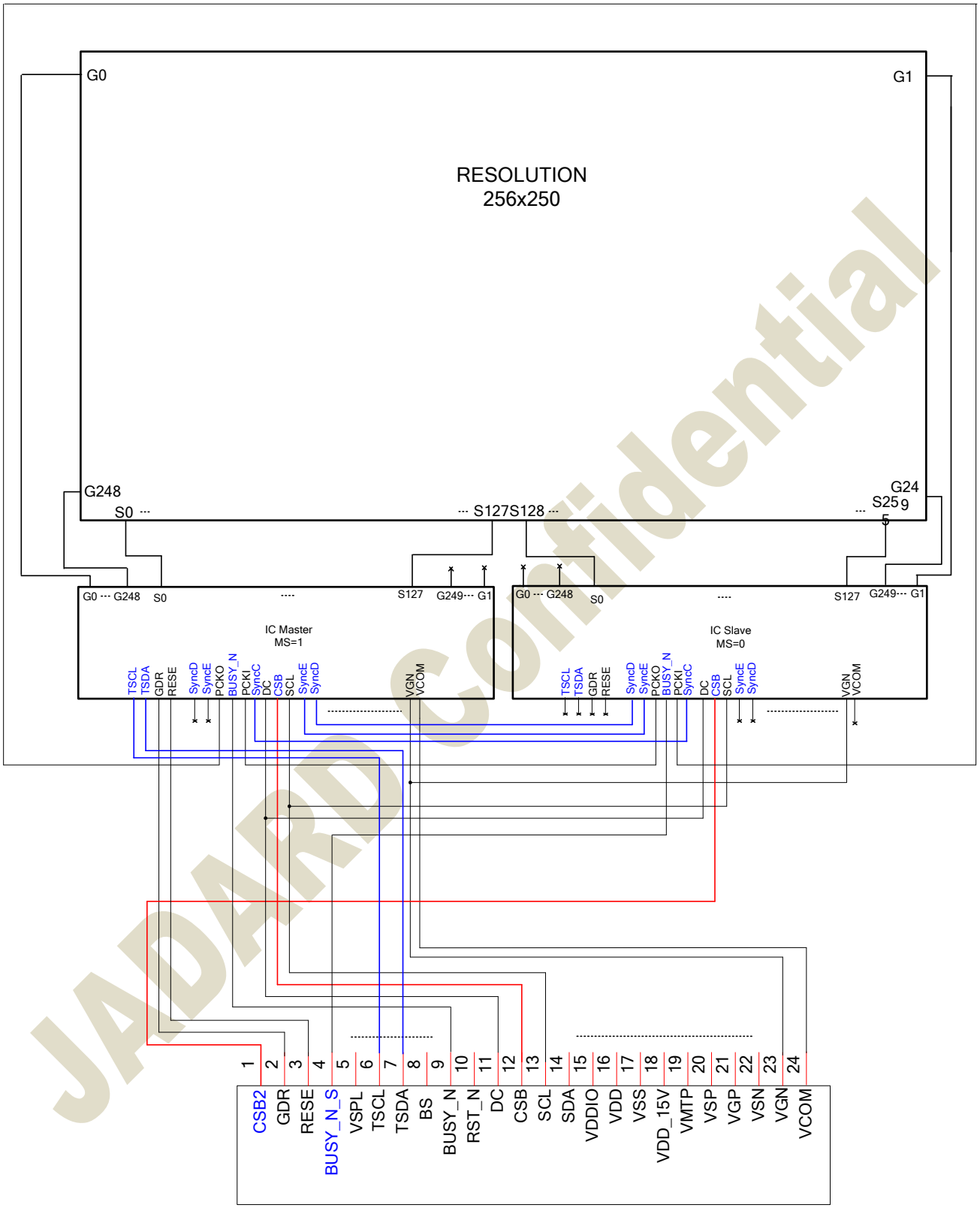
3. BLOCK DIAGRAM



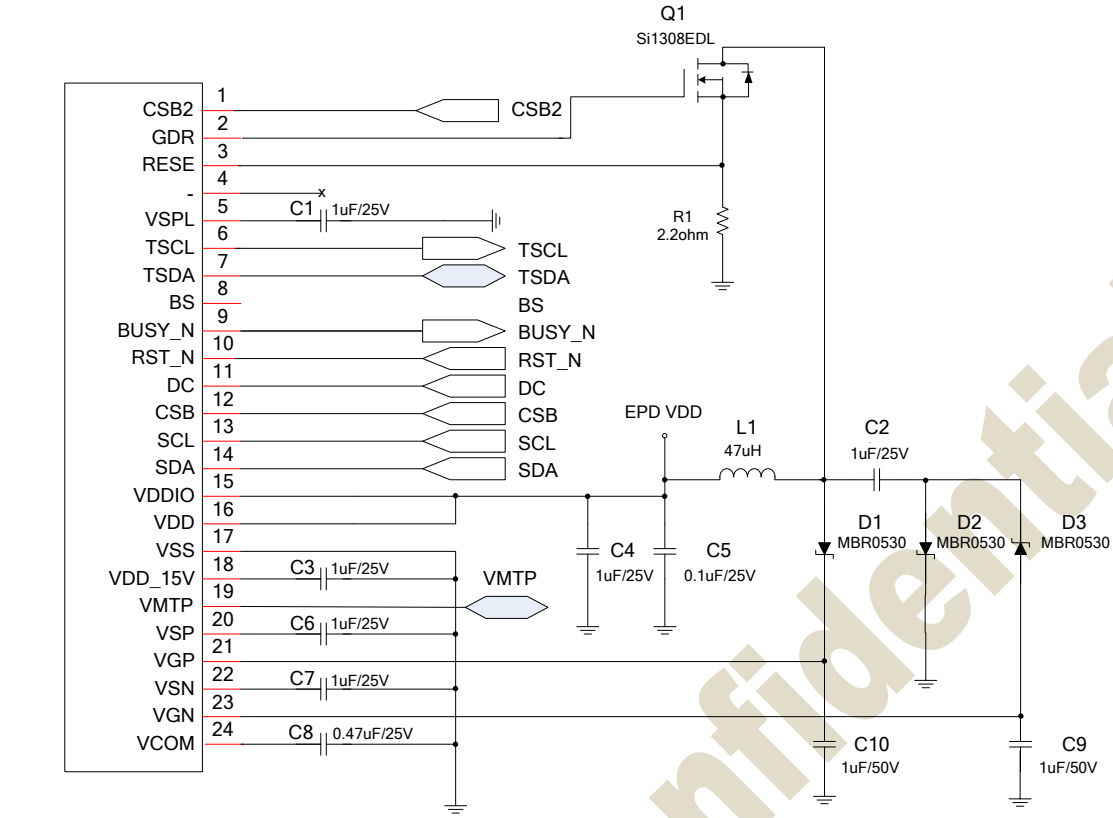
Normal type

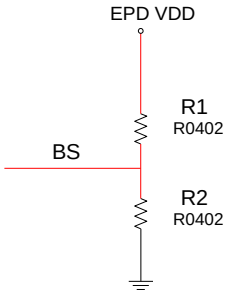


Cascade type (CSB independent / cascade sync with sync_C + sync_D+sync_E)



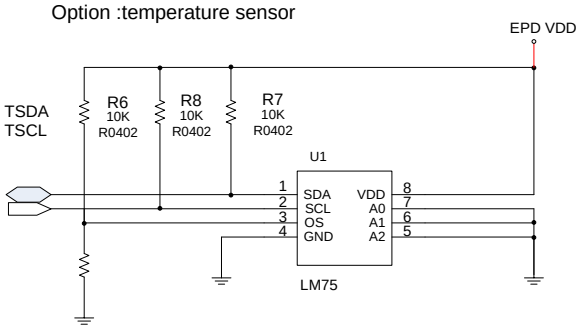
4. APPLICATION CIRCUIT





	R1	R2
3- wire SPI (CSB, SDA, SCL)	10K	NC
4-wire SPI (DC, CSB, SDA, SCL)	NC	10K

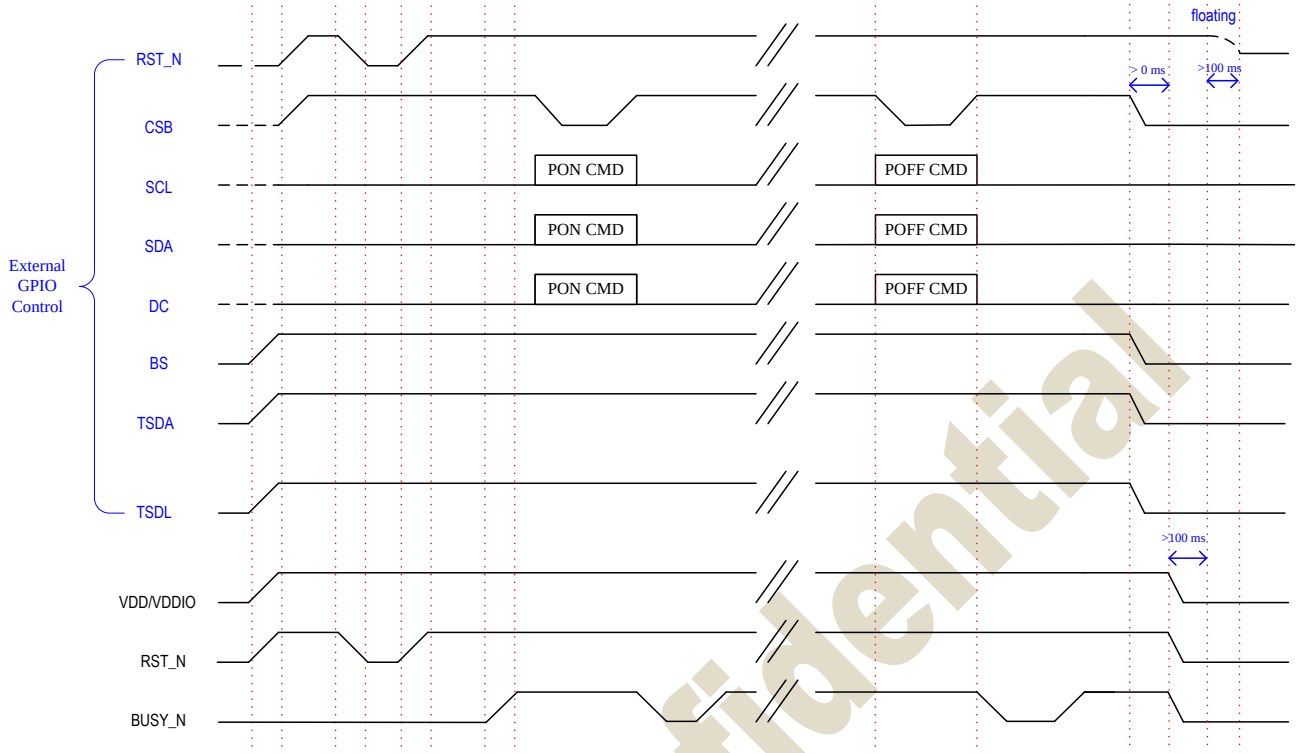
Option :temperature sensor



Reference table of the device:

Device no.	Value	Reference
C1,C2,C3, C4, C6, C7, C8	1uF	0603, X5R/X7R, voltage rating : 25V
C9, C10	1uF	0603, X5R/X7R, voltage rating : 50V
C5	0.1uF	0603, X5R/X7R, voltage rating : 25V
R1	2.2Ω	0603, +/-1% variation
Q1	NMOS	Si1308EDL、Si1304BDL - Drain-source break volatage≧30V - Gate-source threshold voltage≦1.5V - Drain-source on-state resistance<400mΩ
L1	47uH	NR4018T470M、CDRH2D18/LDNP-470NC - Fixed - Maximum DC current~420mA - Maximum DC resistance~650mΩ
D1~D3	Diode	MBR0530 - Reverse DC voltage≧30V - Forward current≧500mA - Forward voltage≦430mV

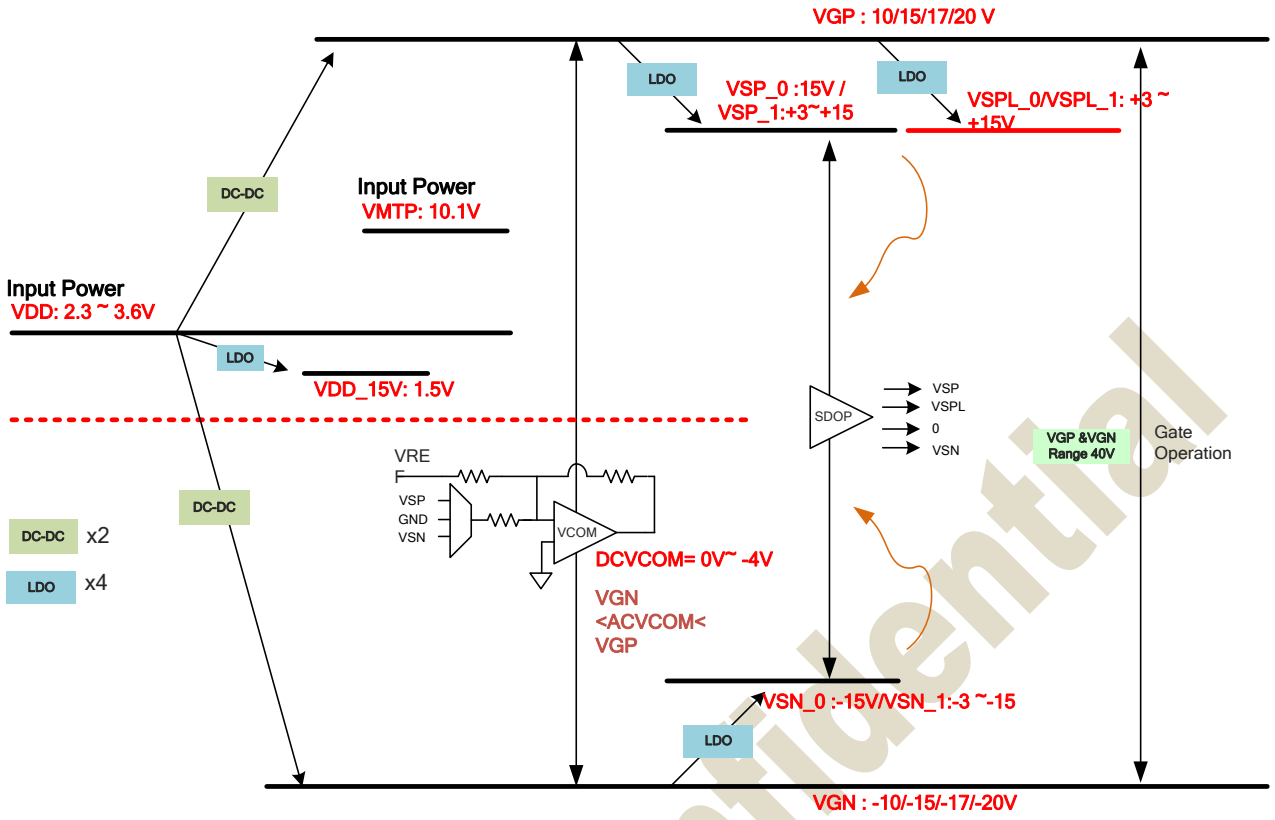
4.1 External GPIO Control



Note:
TSDA: I^2C data for external temperature sensor
TSCL: I^2C clock for external temperature sensor
(I^2C interface need external pull high resistance. Pull low or floating If not used.)

5. APPLICATION POWER CIRCUIT

5.1 Power Generation



6. PIN DESCRIPTION

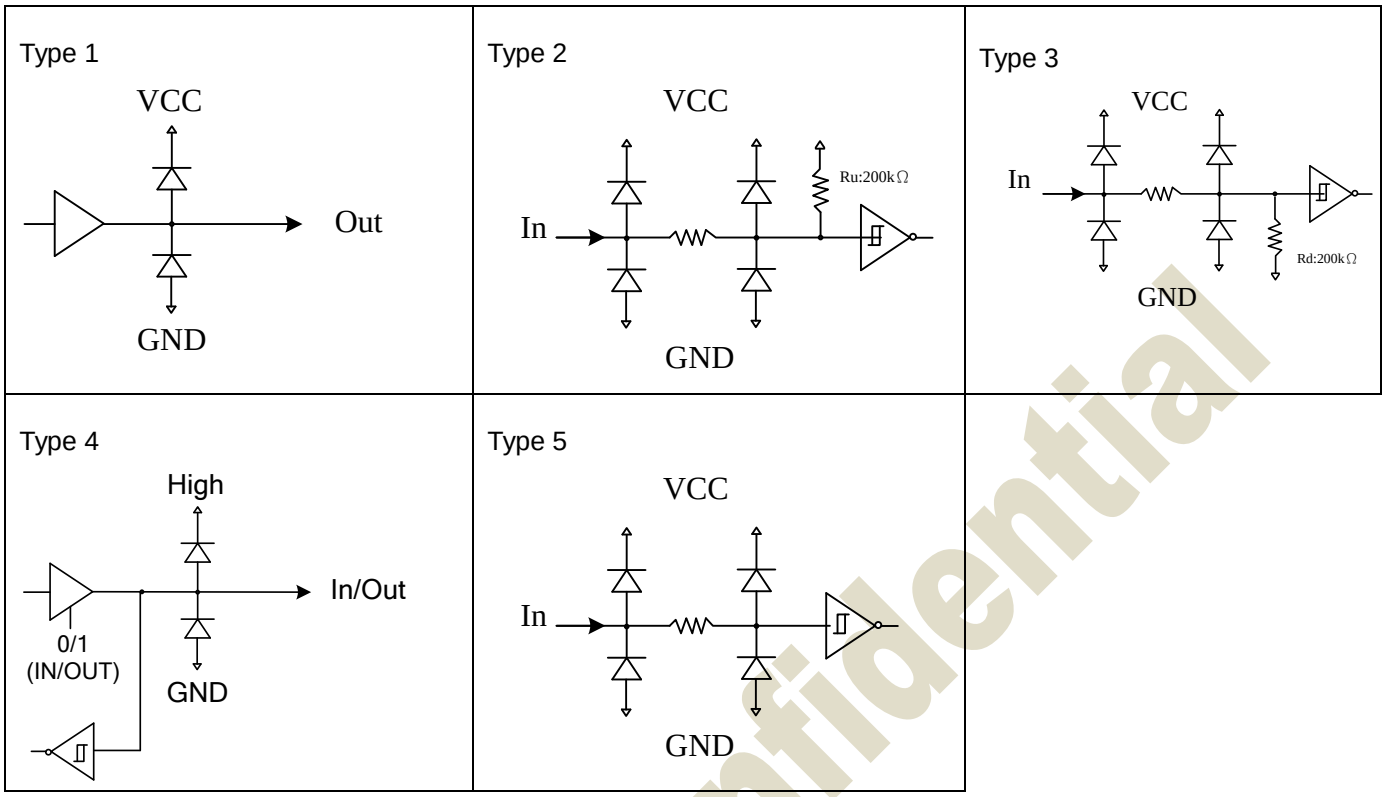
6.1 Pin define

Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 5	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 5	Serial communication clock input.
DC	I	Type 5	Serial communication Command/Data input L: Command H: data Connect to VDD if BS=High.
Control Interface			
RST_N	I	Type 2	Global reset pin. Low reset. (normal pull high) When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will be released to floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= ”0” : Driver is busy, data/VCOM is transforming. BUSY_N= ”1” : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF
TSCL	I/O	Type 4	I^2C clock for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used. (Default low)
TSDA	I/O	Type 4	I^2C data for external temperature sensor (I^2C interface need external pull high resistance.) Must pull high or low if not used.(Default low)
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
Output Driver			
S[127:0]	O	-	Source driver output signals.
G[249:0]	O	-	Gate driver output signals..
Border			
VBD[2:1]	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (-VCM_DC) V 2. (15 +(- VCM_DC)) V or (-15 +(- VCM_DC)) V 3. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.
FB	P	-	Keep open
VGP	P		Positive gate voltage
VGN	P	-	Negative gate voltage.
VSP	P	-	Positive source voltage
VSN	P	-	Negative source voltage.
VSPL	P	-	Positive source voltage

Pin Name	Pin Type	I/O Structure	Description
Power Supply			
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power.
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_15V	P	-	1.5V voltage input &output
VMTP	P	-	MTP program power (10.1V)
Reserved Pins			
T_N18V	I/O	-	Test pin.Leave open or pull gnd.
T_LDON5V	I/O	-	Test pin.Leave open or pull gnd.
T_VCOM	I/O	-	Test pin.Leave open or pull gnd.
T_VSPD_REF	I/O	-	Test pin.Leave open or pull gnd.
T_IBIAS	I/O	-	Test pin.Leave open or pull gnd.
T_VREF	I/O	-	Test pin.Leave open or pull gnd.
T_EN_LSH	I/O	-	Test pin.Leave open or pull gnd.
T_VTSEN	I/O	-	Test pin.Leave open or pull gnd.
T_SAR_REF	I/O	-	Test pin.Leave open or pull gnd.
T_IN[2:0]	I/O	-	Test pin.Leave open or pull gnd.
T_DEBUG[8:0]	I/O	-	Test pin.Leave open or pull gnd.
T_EX_SYSCLK	I/O	-	Test pin.Leave open or pull gnd.
T_EX_REFCLK	I/O	-	Test pin.Leave open or pull gnd.
T_EN_DIG	I/O	-	Test pin.Leave open or pull gnd.
SyncD	I/O	Type 4	Cascade data signal. Leave open or pull gnd if it is not used.
SyncE	I/O	Type 4	Cascade data2 signal. Leave open or pull gnd if it is not used.
SyncC	I/O	Type 4	Cascade clock signal. Leave open or pull gnd if it is not used.
PckI	I	Type 3	Break panel check input. Leave open or gnd if it is not used.
PckO	O	Type 1	Break panel check output. Leave open or gnd if it is not used.
DUMMY[5:0]	D	-	Dummy pin. Leave open or pull gnd.

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

6.2 I/O Pin Structure



6.3 Value of wiring resistance to each pin

Pin name	Wiring resistance value(Ω)	Pin name	Wiring resistance value(Ω)
VCOM	5ohm	TSDA	100ohm
VGP	5ohm	TSCL	100ohm
VGN	5ohm	BS	100ohm
VSP	5ohm	RESE	5ohm
VSN	5ohm	GDR	5ohm
VSPL	5ohm	SDA	100ohm
VMTP	5ohm	SCL	100ohm
VDD_15V	5ohm	CSB	100ohm
VSSA	5ohm	DC	100ohm
VDDIO	5ohm	RST_N	100ohm
VSS	5ohm	SyncE	100ohm
VDDP	5ohm	SyncD	100ohm
VDD	5ohm	SyncC	100ohm
MS	100ohm	PCKI	100ohm
Test pin	100ohm	PCKO	100ohm
BUSY_N	100ohm		

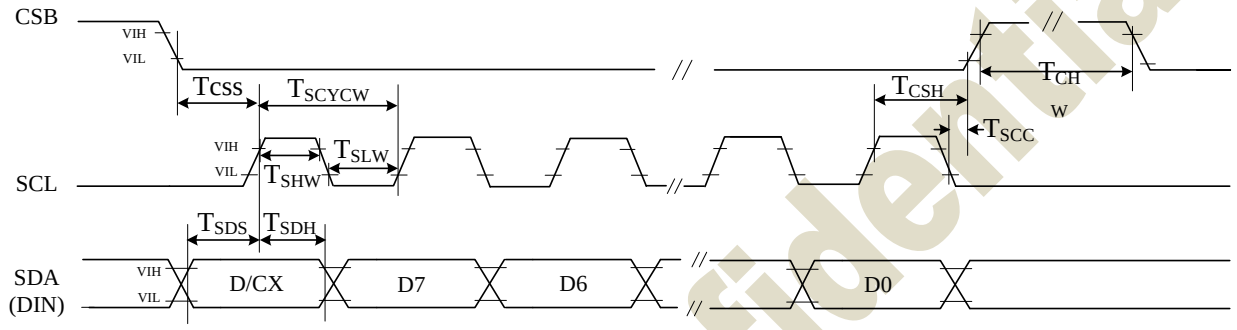
7. SPI COMMAND DESCRIPTION

JD79676 use the 3-wire/4-wire serial port as communication interface for all the function and command setting.

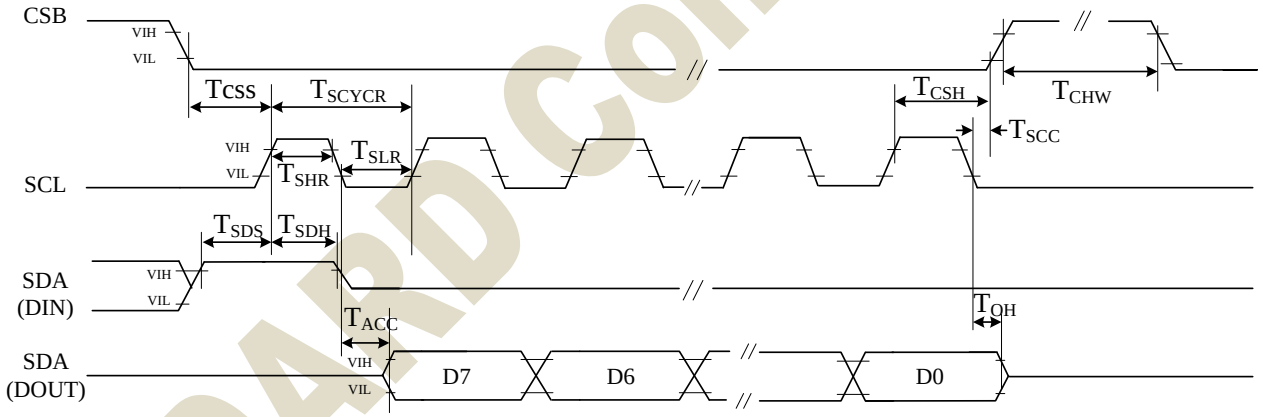
JD79676 3-wire/4-wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

Under read mode, 3-wire/4-wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-wire/4-wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

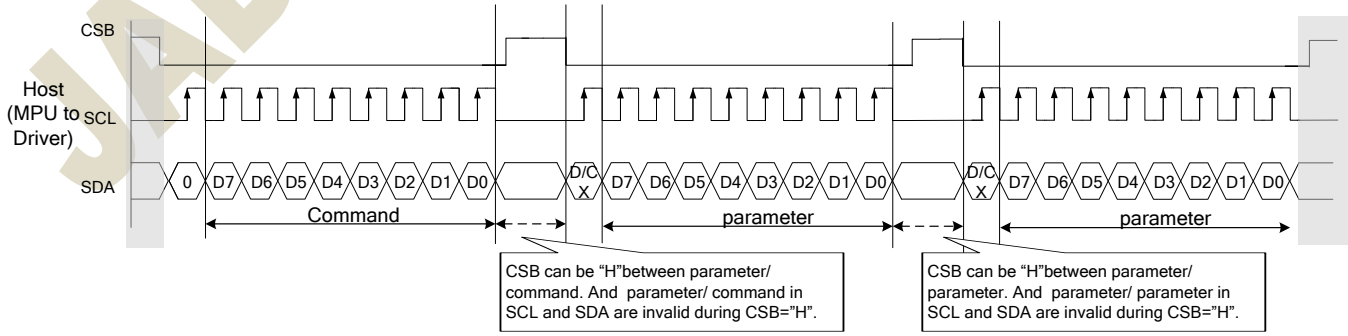
7.1 “3-Wire” Serial Port Interface



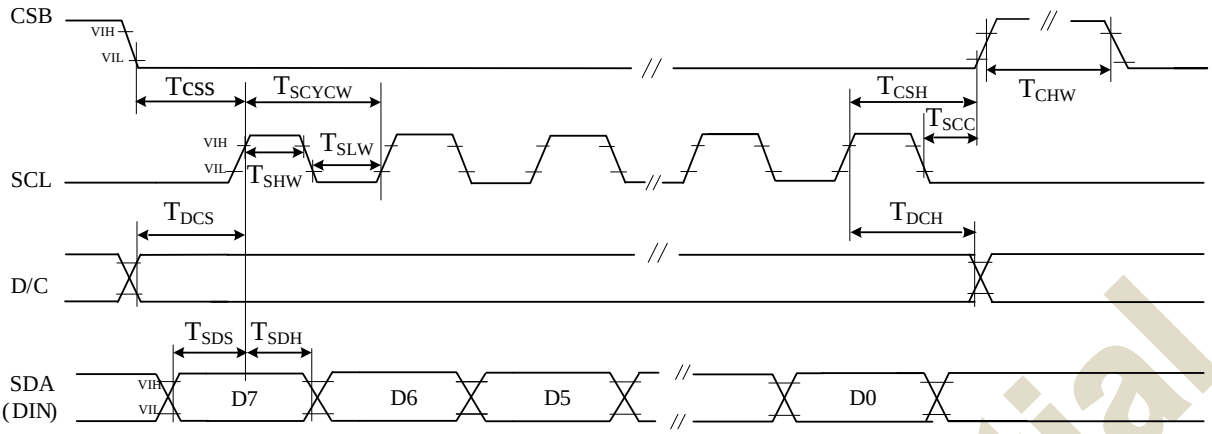
3 pin serial interface characteristics (write mode)



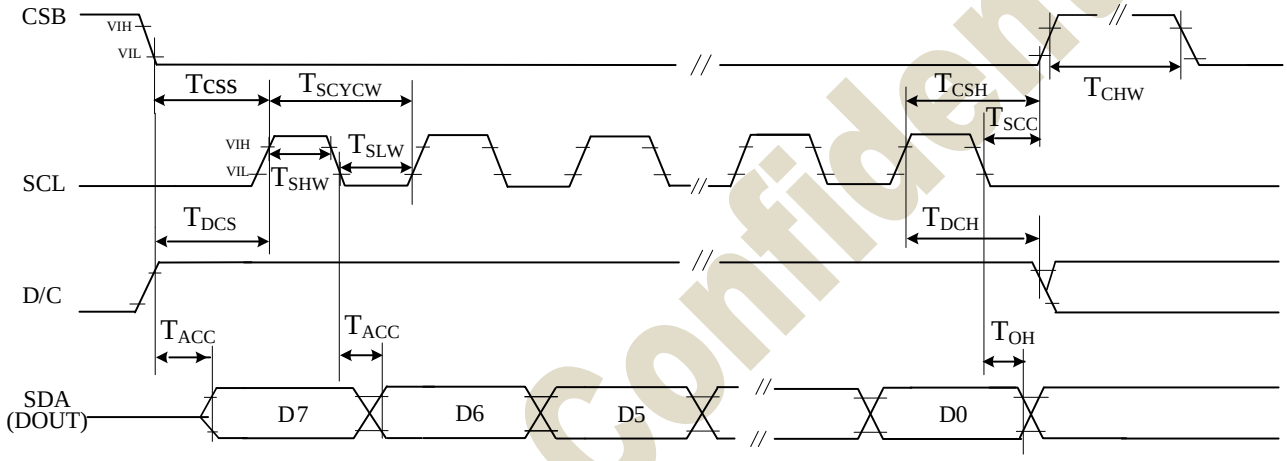
3 pin serial interface characteristics (read mode)



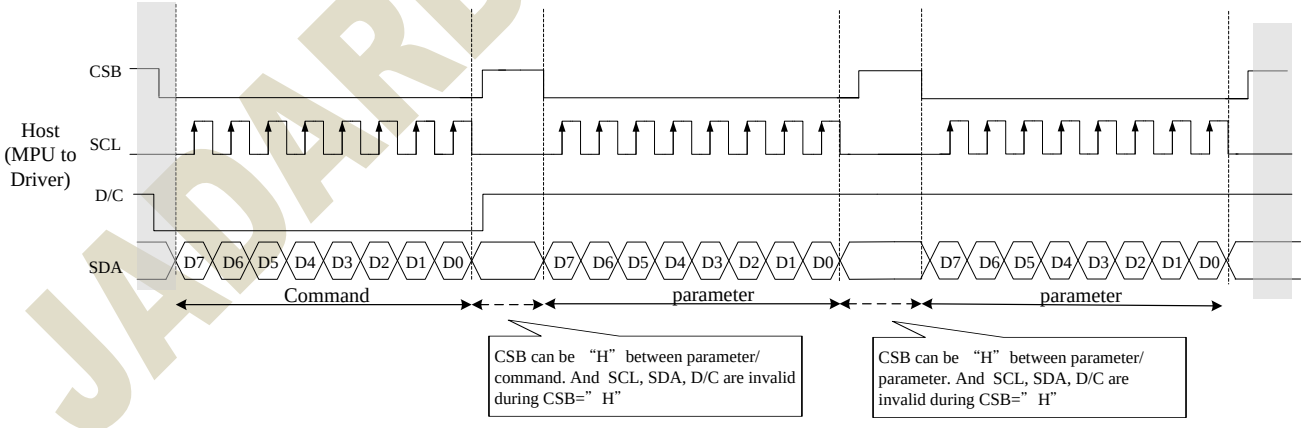
7.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)



8. SPI CONTROL REGISTERS:

8.1 Register Table

Following table list all the SPI control registers and bit name definition for JD79676. Refer to the next section for detail register function description.

Address	command			Bit								
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
		W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-		-	-	VSC_EN	VDS_EN	VDG_EN	07h
		W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
		W	1	-	VSPL_0[6]	VSPL_0[5]	VSPL_0[4]	VSPL_0[3]	VSPL_0[2]	VSPL_0[1]	VSPL_0[0]	00h
		W	1	-	VSP_1[6]	VSP_1 [5]	VSP_1 [4]	VSP_1 [3]	VSP_1 [2]	VSP_1 [1]	VSP_1 [0]	00h
		W	1	-	VSN_1[6]	VSN_1[5]	VSN_1[4]	VSN_1[3]	VSN_1[2]	VSN_1[1]	VSN_1[0]	00h
		W	1	-	VSPL_1[6]	VSPL_1[5]	VSPL_1[4]	VSPL_1[3]	VSPL_1[2]	VSPL_1[1]	VSPL_1[0]	00h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
		W	1	-	-	-	-	-	-	-	-	00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	1	1	0	06H
		W	1	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00h
		W	1	-	-	PHA_ON[5:0]						02h
		W	1	-	-	PHA_OFF[5:0]						07h
		W	1	-	-	PHB_ON[5:0]						02h
		W	1	-	-	PHB_OFF[5:0]						07h
		W	1	-	-	PHC_ON[5:0]						02h
		W	1	-	-	PHC_OFF[5:0]						07h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission (DTM)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	--
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
		W	1	-	-	-	-	-	-	-	-	00H
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	-	-	-	Dyna		FR[2:0]		02h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[7]	D8/TS[6]	D7/TS[5]	D6/TS[4]	D5/TS[3]	D4/TS[2]	D3/TS[1]	--
		R	1	D2/ TS[9]	D1/TS[8]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
		R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	--
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[2]	VBD[1]	VBD[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	--
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R65H	Gate/Source Start Setting(GSST)	W	0	0	1	1	0	0	1	0	1	65H
		W	1	-	-	-	-	-	-	S_start(9)	S_start(8)	00h
		W	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00h
		W	1	-	-	-	-	-	-	G_start(9)	G_start(8)	00h
		W	1	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	0	0	0	0	1	0	0	1	09h
		R	1	0	0	0	0	0	0	1	0	02h
		R	1	0	0	0	0	0	0	0	1	01h
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h
R83H	Partial Window (PTLW)	W	0	1	0	0	0	0	0	1	1	83H
		W	1	-	-	-	PTH_ENB	-	-	HRST(9)	HRST(8)	00h
		W	1	HRST(7)	HRST(6)	HRST(5)	HRST(4)	HRST(3)	HRST(2)	0	0	00h
		W	1	-	-	-	-	-	-	HRED(9)	HRED(8)	00h
		W	1	HRED(7)	HRED(6)	HRED(5)	HRED(4)	HRED(3)	HRED(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	-	PMOD	00h
R90H	Program mode(PGM)	W	0	1	0	0	1	0	0	0	0	90H
R91H	Active Program(APG)	W	0	1	0	0	1	0	0	0	1	91H
R92H	Read MTP data (RMTP)	W	0	1	0	0	1	0	0	1	0	92H
		R	1	#	#	#	#	#	#	#	#	-
RA2H	MTP Program Config Register(PGM_CFG)	W	0	1	0	1	0	0	0	1	0	A2H
		W	1	-	-	-	VMTPSEL	-	-	M_dis	S_dis	00h
		W	1	PGM_SADDR[15:8]								00h
		W	1	PGM_SADDR[7:0]								00h
		W	1	PGM_DSIZE[15:8]								0Fh
		W	1	PGM_DSIZE[7:0]								00h
RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H
		W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h
RE3H	Power saving(PWS)	W	0	1	1	1	0	0	0	1	1	E3H
		W	1	VCOM_W [3]	VCOM_W [2]	VCOM_W [1]	VCOM_W [0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h
RE4H	LVD voltage Select(LVSEL)	W	0	1	1	1	0	0	1	0	0	E4H
		W	1	-	-	-	-	-	-	LVD_SEL [1]	LVD_SEL [0]	03h
RE5H	CASCADE setting select (CCS_SEL)	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	-	-	-	-	cascade_sync	-	-	-	00h

8.2 Register Description

R/W: 0:Write Cycle 1:Read Cycle
D/CX:0:Command/1:Data
D7~D0:-:Don't Care

8.2.1R00H (PSR): Panel setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2nd Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st parameter

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and Source / Border / Vcom are kept 0V or floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →…→S2→Last data=S1. 1: Shift right: First data=S1→S2 →…→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →…→G2→Last line=G1. 1:Scan up; First line=G1→G2 →…→Gn-1→Last line=Gn. (default)
5	PST_MODE	Power switch operation mode 0:Power switching time in the period of frame scanning.(default) 1:Power switching time in the external period before frame scanning.
7-6	RES[1,0]	Resolution setting 00: Display resolution is 128x250(default) 01: Display resolution is 96x250 10: Display resolution is 64x250 11: Display resolution is 32x250

2nd parameter

Bit	Name	Description
0	VC_LUTZ	VCOM status function 0 : No effect 1 : After refreshing display, the output of VCOM is set to floating automatically (default)
1	NORG	VCOM status function 0 : No effect (default) 1 : After refreshing display, VCOM is tied to GND before power off
2	TIEG	VGN power off status function 0 : No effect (default) 1 : Power off, VGN will be tied to GND
3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling booster,Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high,Temperature Sensor will be activated automatically one time. (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	FOPT	FOPT function 0: Scan 1 frame after waveform finished(default) 1: No scan after waveform finished and switch the source channel output to Hiz.
7	LUT_EN	LUT selection setting 0 : Using LUT from MTP(default) 1 : Using LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.
FOPT: Power off floating.

Notes:
1. Non-select gate line keep at VGN for DSP/DRF and AMV
2. Dummy source line follow LUTC for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off.SD output and VCOM will base on previous condition. It may have two condition:0V or floating.
4. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. Source/Gate/Border/VCOM will be released to floating

Restriction	

8.2.2 R01H (PWR): Power setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07h
2nd Parameter	W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
3rd Parameter	W	1	-	VSPL_0 [6:0]							00h
4th Parameter	W	1	-	VSP_1 [6:0]							00h
5th Parameter	W	1	-	VSN_1 [6:0]							00h
6th Parameter	W	1	-	VSPL_1 [6:0]							00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	Gate power selection. 0 : External gate power from VGP/VGN pins. 1 : Internal DCDC function for generate VGP/VGN. (default)
1	VDS_EN	Source power selection. 0 : External source power from VSP/VSN pins. 1 : Internal regulator function for generate VSP/VSN (default)
2	VSC_EN	Source LV power selection. 0 : External source power from VSPL pins. 1 : Internal regulator function for generate VSPL (default)

2nd Parameter:

Bit	Name	Description
1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v

3rd & 4th & 6th Parameter: Internal VSP_1/VSPL_0/ VSPL_1 power selection

Bit	Name	Description
6-0	VSP_1 & VSPL_0 & VSPL_1	**Internal VSP & VSPL power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	3	0101001	29h	7.1	1010010	52h	11.2
0000001	01h	3.1	0101010	2Ah	7.2	1010011	53h	11.3
0000010	02h	3.2	0101011	2Bh	7.3	1010100	54h	11.4
0000011	03h	3.3	0101100	2Ch	7.4	1010101	55h	11.5
0000100	04h	3.4	0101101	2Dh	7.5	1010110	56h	11.6
0000101	05h	3.5	0101110	2Eh	7.6	1010111	57h	11.7
0000110	06h	3.6	0101111	2Fh	7.7	1011000	58h	11.8
0000111	07h	3.7	0110000	30h	7.8	1011001	59h	11.9
0001000	08h	3.8	0110001	31h	7.9	1011010	5Ah	12
0001001	09h	3.9	0110010	32h	8	1011011	5Bh	12.1
0001010	0Ah	4	0110011	33h	8.1	1011100	5Ch	12.2
0001011	0Bh	4.1	0110100	34h	8.2	1011101	5Dh	12.3
0001100	0Ch	4.2	0110101	35h	8.3	1011110	5Eh	12.4
0001101	0Dh	4.3	0110110	36h	8.4	1011111	5Fh	12.5
0001110	0Eh	4.4	0110111	37h	8.5	1100000	60h	12.6
0001111	0Fh	4.5	0111000	38h	8.6	1100001	61h	12.7
0010000	10h	4.6	0111001	39h	8.7	1100010	62h	12.8
0010001	11h	4.7	0111010	3Ah	8.8	1100011	63h	12.9
0010010	12h	4.8	0111011	3Bh	8.9	1100100	64h	13
0010011	13h	4.9	0111100	3Ch	9	1100101	65h	13.1
0010100	14h	5	0111101	3Dh	9.1	1100110	66h	13.2
0010101	15h	5.1	0111110	3Eh	9.2	1100111	67h	13.3
0010110	16h	5.2	0111111	3Fh	9.3	1101000	68h	13.4
0010111	17h	5.3	1000000	40h	9.4	1101001	69h	13.5
0011000	18h	5.4	1000001	41h	9.5	1101010	6Ah	13.6
0011001	19h	5.5	1000010	42h	9.6	1101011	6Bh	13.7
0011010	1Ah	5.6	1000011	43h	9.7	1101100	6Ch	13.8
0011011	1Bh	5.7	1000100	44h	9.8	1101101	6Dh	13.9
0011100	1Ch	5.8	1000101	45h	9.9	1101110	6Eh	14
0011101	1Dh	5.9	1000110	46h	10	1101111	6Fh	14.1
0011110	1Eh	6	1000111	47h	10.1	1110000	70h	14.2
0011111	1Fh	6.1	1001000	48h	10.2	1110001	71h	14.3
0100000	20h	6.2	1001001	49h	10.3	1110010	72h	14.4
0100001	21h	6.3	1001010	4Ah	10.4	1110011	73h	14.5
0100010	22h	6.4	1001011	4Bh	10.5	1110100	74h	14.6
0100011	23h	6.5	1001100	4Ch	10.6	1110101	75h	14.7
0100100	24h	6.6	1001101	4Dh	10.7	1110110	76h	14.8
0100101	25h	6.7	1001110	4Eh	10.8	1110111	77h	14.9
0100110	26h	6.8	1001111	4Fh	10.9	1111000	78h	15
0100111	27h	6.9	1010000	50h	11	other		15
0101000	28h	7	1010001	51h	11.1			

5th Parameter: Internal VSN_1 power selection

Bit	Name	Description
6-0	VSN_1	**Internal VSN power selection.**

bit[6:0]		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		Voltage(V)
0000000	00h	-3	0101001	29h	-7.1	1010010	52h	-11.2
0000001	01h	-3.1	0101010	2Ah	-7.2	1010011	53h	-11.3
0000010	02h	-3.2	0101011	2Bh	-7.3	1010100	54h	-11.4
0000011	03h	-3.3	0101100	2Ch	-7.4	1010101	55h	-11.5
0000100	04h	-3.4	0101101	2Dh	-7.5	1010110	56h	-11.6
0000101	05h	-3.5	0101110	2Eh	-7.6	1010111	57h	-11.7
0000110	06h	-3.6	0101111	2Fh	-7.7	1011000	58h	-11.8
0000111	07h	-3.7	0110000	30h	-7.8	1011001	59h	-11.9
0001000	08h	-3.8	0110001	31h	-7.9	1011010	5Ah	-12
0001001	09h	-3.9	0110010	32h	-8	1011011	5Bh	-12.1
0001010	0Ah	-4	0110011	33h	-8.1	1011100	5Ch	-12.2
0001011	0Bh	-4.1	0110100	34h	-8.2	1011101	5Dh	-12.3
0001100	0Ch	-4.2	0110101	35h	-8.3	1011110	5Eh	-12.4
0001101	0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh	-12.5
0001110	0Eh	-4.4	0110111	37h	-8.5	1100000	60h	-12.6
0001111	0Fh	-4.5	0111000	38h	-8.6	1100001	61h	-12.7
0010000	10h	-4.6	0111001	39h	-8.7	1100010	62h	-12.8
0010001	11h	-4.7	0111010	3Ah	-8.8	1100011	63h	-12.9
0010010	12h	-4.8	0111011	3Bh	-8.9	1100100	64h	-13
0010011	13h	-4.9	0111100	3Ch	-9	1100101	65h	-13.1
0010100	14h	-5	0111101	3Dh	-9.1	1100110	66h	-13.2
0010101	15h	-5.1	0111110	3Eh	-9.2	1100111	67h	-13.3
0010110	16h	-5.2	0111111	3Fh	-9.3	1101000	68h	-13.4
0010111	17h	-5.3	1000000	40h	-9.4	1101001	69h	-13.5
0011000	18h	-5.4	1000001	41h	-9.5	1101010	6Ah	-13.6
0011001	19h	-5.5	1000010	42h	-9.6	1101011	6Bh	-13.7
0011010	1Ah	-5.6	1000011	43h	-9.7	1101100	6Ch	-13.8
0011011	1Bh	-5.7	1000100	44h	-9.8	1101101	6Dh	-13.9
0011100	1Ch	-5.8	1000101	45h	-9.9	1101110	6Eh	-14
0011101	1Dh	-5.9	1000110	46h	-10	1101111	6Fh	-14.1
0011110	1Eh	-6	1000111	47h	-10.1	1110000	70h	-14.2
0011111	1Fh	-6.1	1001000	48h	-10.2	1110001	71h	-14.3
0100000	20h	-6.2	1001001	49h	-10.3	1110010	72h	-14.4
0100001	21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5
0100010	22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6
0100011	23h	-6.5	1001100	4Ch	-10.6	1110101	75h	-14.7
0100100	24h	-6.6	1001101	4Dh	-10.7	1110110	76h	-14.8
0100101	25h	-6.7	1001110	4Eh	-10.8	1110111	77h	-14.9
0100110	26h	-6.8	1001111	4Fh	-10.9	1111000	78h	-15
0100111	27h	-6.9	1010000	50h	-11	other		-15
0101000	28h	-7	1010001	51h	-7.1			

Notes:

1. VSP_0/VSN_0 voltage output is ±15 V fixed value.
2. When switching Mode0 or Mode1,the voltage output is:
   Mode0: VSP_0(+15) / VSN_0 (-15) / VSPL_0 (+3~+15)
   Mode1: VSP_1(+3 ~ +15) / VSN_1(-3 ~ -15) / VSPL_1(+3 ~ +15)

	Mode0	Mode1
VSP	VSP_0(+15)	VSP_1(+3~+15)
VSN	VSN_0(-15)	VSN_1(-3~-15)
VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)

3. If gate voltage is set to +/-15v, +/-10v, IC will auto correct source voltage as follows
   I. VGP- VSP_0 / VSPL_0 / VSP_1 / VSPL_1 >= 2v
   II. VGN- VSN_0 / VSN_1 >= -2v
   For example:

	symbol	Voltage setting	Real Voltage
Voltage	VGP	+10v	+10v
	VGN	-10v	-10v
	VSP_0	+15v	+8v
	VSN_0	-15v	-8v
	VSP_1	+5v	+5v
	VSN_1	-5v	-5v
	VSPL	+15v	+8v
	VCOMH	+15v+(-2v)	+8v +(-2v)
	VCOML	-15v+(-2v)	-8v +(-2v)
	VCOMDC	-2v	-2v

Restriction	

8.2.3 R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H
1st Parameter	W	0	-	-	-	-	-	-	-	-	00

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N singal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

8.2.4 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence (base on PWR command), BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

8.2.5 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	-	-	-	-	PHB_SFT [1:0]		PHA_SFT [1:0]		00h
2nd Parameter	W	1	-	-	PHA_ON [5:0]						02h
3rd Parameter	W	1	-	-	PHA_OFF [5:0]						07h
4th Parameter	W	1	-	-	PHB_ON [5:0]						02h
5th Parameter	W	1	-	-	PHB_OFF [5:0]						07h
6th Parameter	W	1	-	-	PHC_ON [5:0]						02h
7th Parameter	W	1	-	-	PHC_OFF [5:0]						07h

Description

-The command define as follows:

Boost Current mode and Constant On Time mode setting by JD CMD

1st Parameter:

Bit	Name	Description
1-0	PHA_SFT	Soft start period of phase A: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS
3-2	PHB_SFT	Soft start period of phase B: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Driving strength of PHA_ON & PHB_ON & PHC_ON	000000	strength1	010110	strength23	101100	strength45
	000001	strength2	010111	strength24	101101	strength46
	000010	strength3	011000	strength25	101110	strength47
	000011	strength4	011001	strength26	101111	strength48
	000100	strength5	011010	strength27	110000	strength49
	000101	strength6	011011	strength28	110001	strength50
	000110	strength7	011100	strength29	110010	strength51
	000111	strength8	011101	strength30	110011	strength52
	001000	strength9	011110	strength31	110100	strength53
	001001	strength10	011111	strength32	110101	strength54
	001010	strength11	100000	strength33	110110	strength55
	001011	strength12	100001	strength34	110111	strength56
	001100	strength13	100010	strength35	111000	strength57
	001101	strength14	100011	strength36	111001	strength58
	001110	strength15	100100	strength37	111010	strength59
	001111	strength16	100101	strength38	111011	strength60
	010000	strength17	100110	strength39	111100	strength61
	010001	strength18	100111	strength40	111101	strength62
	010010	strength19	101000	strength41	111110	strength63
	010011	strength20	101001	strength42	111111	strength64
	010100	strength21	101010	strength43		
	010101	strength22	101011	strength44		

Description

	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Minimum OFF time setting of PHA_OFF & PHB_OFF & PHC_OFF	000000	Period1	010110	Period23	101100	Period45
	000001	Period2	010111	Period24	101101	Period46
	000010	Period3	011000	Period25	101110	Period47
	000011	Period4	011001	Period26	101111	Period48
	000100	Period5	011010	Period27	110000	Period49
	000101	Period6	011011	Period28	110001	Period50
	000110	Period7	011100	Period29	110010	Period51
	000111	Period8	011101	Period30	110011	Period52
	001000	Period9	011110	Period31	110100	Period53
	001001	Period10	011111	Period32	110101	Period54
	001010	Period11	100000	Period33	110110	Period55
	001011	Period12	100001	Period34	110111	Period56
	001100	Period13	100010	Period35	111000	Period57
	001101	Period14	100011	Period36	111001	Period58
	001110	Period15	100100	Period37	111010	Period59
	001111	Period16	100101	Period38	111011	Period60
	010000	Period17	100110	Period39	111100	Period61
	010001	Period18	100111	Period40	111101	Period62
	010010	Period19	101000	Period41	111110	Period63
	010011	Period20	101001	Period42	111111	Period64
	010100	Period21	101010	Period43		
	010101	Period22	101011	Period44		

Restriction

8.2.6 R07H (DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

8.2.7 R10H (DTM): Data Start transmission Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM_master	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h
: :	W	1	: :		: :		: :		: :		00h
Mth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 12H. Then chip will start to send data/VCOM for panel.

Pixel [1~n][1:0]: 2-bit/pixel

Image Data	DDX=1(default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00b	Gray0	ogray00	Gray3	ogray03
01b	Gray1	ogray01	Gray2	ogray02
10b	Gray2	ogray02	Gray1	ogray01
11b	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1,Pixel[1:0]=01 ->Gray level select=Gray1,follow LUT data output from IP output port"ogray01".

When DDX=0,Pixel[1:0]=11 ->Gray level select=Gray0,follow LUT data output from IP output port"ogray00"

Restriction

8.2.8 R11H (DSP): Data Stop Command

R11H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSP	W	0	0	0	0	1	0	0	0	1	11H
1st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ While finished the data transmitting, user must send this command to driver and read Data_flag information. 1st Parameter: Bit / Name / Description 7 / Data_flag / 0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data. After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.
Restriction	This command only actives when BUSY_N = "1".

8.2.9 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H
1st Parameter	W	1	-	-	-	-	-	-	-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : R12h=0x00 While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0"
Restriction	This command only actives when BUSY_N = "1"

8.2.10 R17H (AUTO): Auto Sequence

R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code(0xA5) = (PON→DRF→POF) AUTO (0x17) + Code(0xA7) = (PON→DRF→POF→DSLP)
Restriction	This command only actives when BUSY_N = "1".

8.2.11 R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	02h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

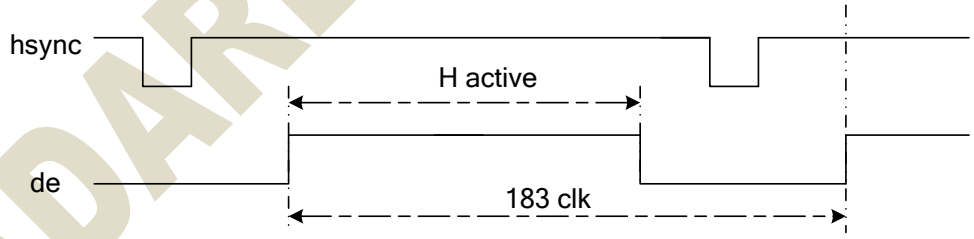
bit3	Dynamic frame rate
0	Disable(default)
1	Enable

Note:
Dynamic frame rate
0: Frame rate will being defined in R30h.
1: Frame rate will being defined by R20h(LUT).

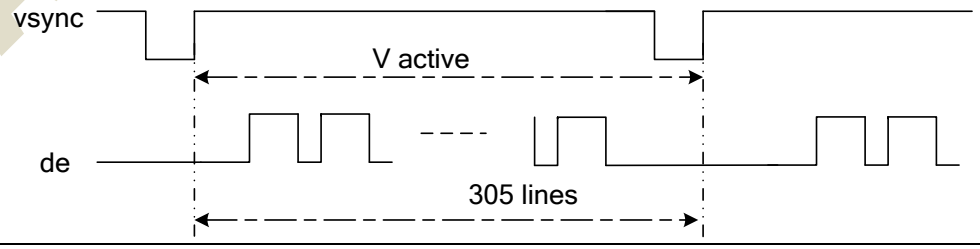
FR[2:0]	Frame rate
000	12.5 Hz
001	25 Hz
010	50 Hz(default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

remark

-Horizental



-Vertical



Restriction

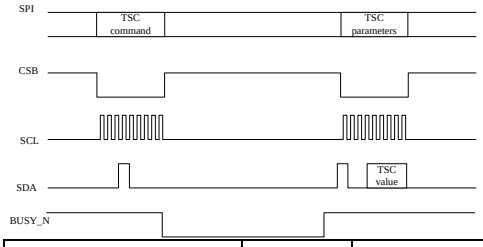
8.2.12 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	-
2nd Parameter	R	1	D2/ TS[9]	D1/ TS[8]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:
This command indicates the temperature value.
If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.
If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[9:8]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction: This command only actives when BUSY_N = "1".

8.2.13 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Reserve one temperature offset TO[3:0] for calibration
1. TO[3]: mean '+' or '-' , while 0 is '+' ; 1 is '-'
2. TO[2:0]: mean temperature offset value

Bit	Name	Description
3-0	TO[3:0]	Temperature level: 0000: +0℃ (default) 0001: +0.5℃ 0010: +1℃ 0011: +1.5℃ 0100: +2℃ 0101: +2.5℃ 0110: +3℃ 0111: +3.5℃ 1000: -4℃ 1001: -3.5℃ 1010: -3℃ 1011: -2.5℃ 1100: -2℃ 1101: -1.5℃ 1110: -1℃ 1111: -0.5℃
4	TO[4]	0: +0.0℃ (default) 1: +0.25℃
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

Restriction: This command only actives after R04H(PON)

8.2.14 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command writes the temperature.

1st Parameter:

Bit	Name	Description
2-0	WATTR[2:0]	Pointer setting
5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)
7-6	WATTR[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

2nd Parameter:

Bit	Name	Description
7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor

3nd Parameter:

Bit	Name	Description
7-0	WLSB[7:0]	LSByte of write-data to external temperature sensor

Restriction: This command only actives after R04H(PON)

8.2.15 R43H (TSR): Temperature Sensor Read Register

R43H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSR	W	0	0	1	0	0	0	0	1	1	43H
1st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-
2nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

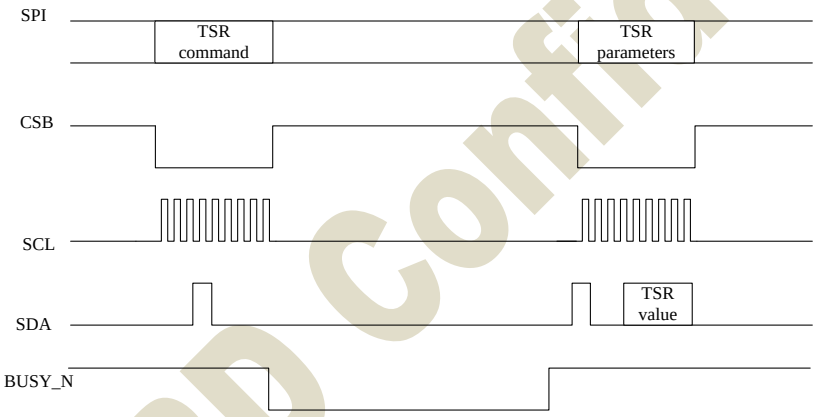
This command reads the temperature sensed by the temperature sensor.

1st Parameter:

Bit	Name	Description
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor

2nd Parameter:

Bit	Name	Description
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor



Restriction: This command only actives after R04H(PON)

8.2.16 R50H (CDI): VCOM and DATA interval setting Register

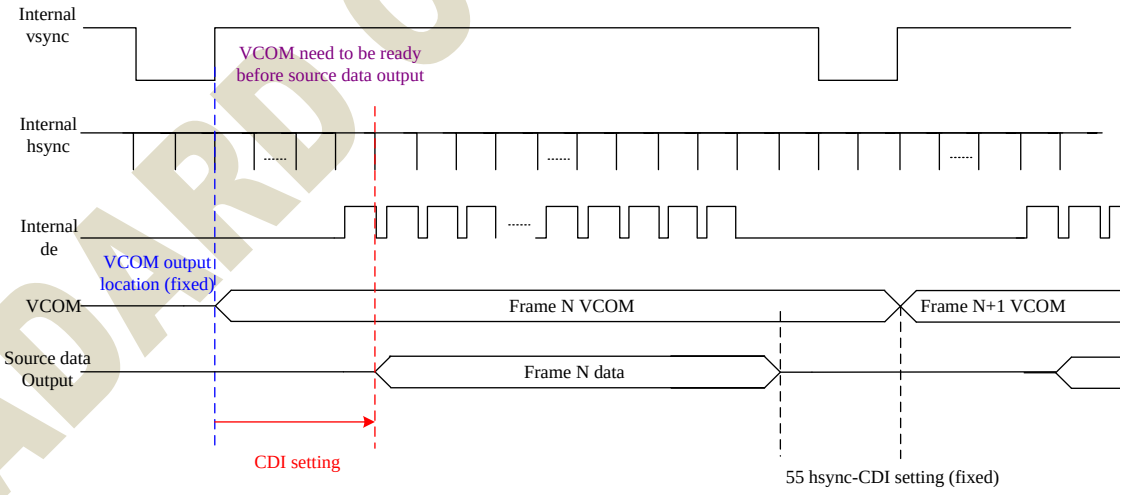
R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[2]	VBD[1]	VBD [0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command can set 2 kinds of parameters, 1.VCOM to data output interval(CDI)
:
CDI[3:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (55hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync(default) 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[2:0]: Border data selection. (from LUT output by IP port border_w[1:0])

This register will make boarder pin output being mapped to a certain gray scale.

Bit 4	Bit7-5	Description	IP setting for Border LUT select
DDX	VBD[2:0]	Gray level	
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating	N/A

Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V, without VCOM offset, the real output on Boarder pin shall be 15V.

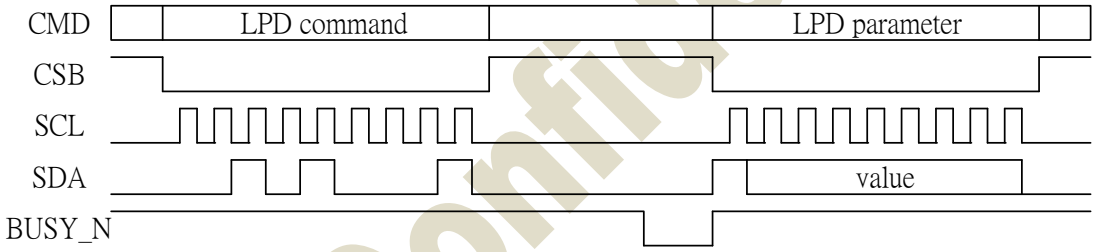
Boarder output will follow FOPT definition being defined in R00h.

Restriction	

8.2.17 R51H (LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)). 1st Parameter: Bit 0 / LPD 0 / Low power input. 1 / Normal status. 
Restriction	This command only actives when BUSY_N = "1".

8.2.18 R61H (TRES): Resolution setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
3th Parameter	W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES Note: No matter HRES[9:8],HRES[1:0],VRES[9:8] value being filled, it's always be 00b. Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[9:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:2]*4-1 EX :128x250 GD: First G active = G0 LAST active GD= 0+250-1= 249; (G249) SD : First active channel: =S0 LAST active SD=0+32*4-1=127; (S127)
Restriction	Horizontal resolution should be 4-multiple.

8.2.19 R65H (GSST): Gate/Source Start Setting Register

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1st Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2nd Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h
3rd Parameter	W	1	-				-	-	G_start[9]	G_start[8]	00h
4th Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: Note: No matter S_start[9:8], S_start [1:0], G_start [9:8] value being filled, it's always be 00b. 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line
Restriction	S_Start should be the multiple of 4

8.2.20 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	0	0	0	0	1	0	0	1	09h
2nd Parameter	R	1	0	0	0	0	0	0	1	0	02h
3rd Parameter	R	1	0	0	0	0	0	0	0	1	01h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: 1st & 2nd & 3rd Parameter:

Bit	Description
7-0	CHIP_REV

Restriction	

8.2.21 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h

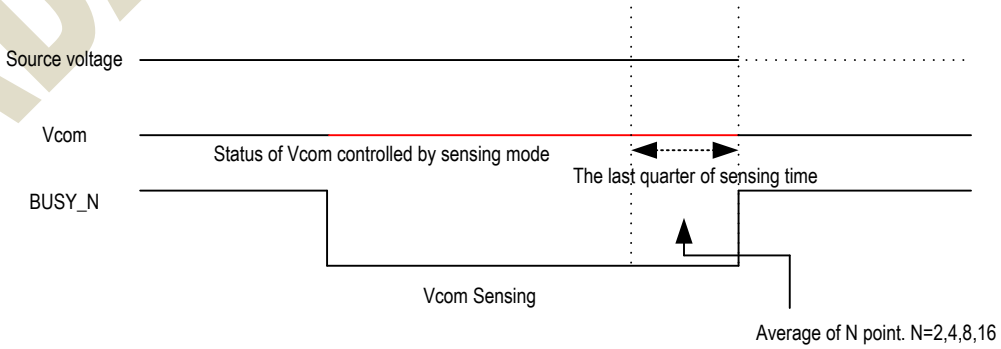
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSPL_0 during Auto Measure VCOM period.
3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 5s (default) 01: 10s 10: 15s 11: 20s
7-6	P[1:0]	The sensing points of sampling time 00: 2 (default) 01: 4 10: 8 11: 16 Sampling time = the last quarter of sensing time (T) VCOM = average of N points. N=2,4,8,16



Restriction: This command only actives when BUSY_N = "1".

8.2.22 R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter:

Bit	Name	Description
6-0	VV[6:0]	**VCOM value**

VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)	VV [6:0]		Voltage(V)
0000000	00h	0	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

Restriction

8.2.23 R82H (VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	VDCS[6]	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.
1st Parameter:

Bit	Name	Description
6-0	VDCS[6:0]	**VCOM value**

VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)	VDCS [6:0]		Voltage(V)
0000000	00h	0(default)	0011100	1Ch	-1.4	0111000	38h	-2.8
0000001	01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
0000010	02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
0000011	03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
0000100	04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
0000101	05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
0000110	06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
0000111	07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
0001000	08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
0001001	09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
0001010	0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
0001011	0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
0001100	0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4
0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
0011001	19h	-1.25	0110101	35h	-2.65	other		-4
0011010	1Ah	-1.3	0110110	36h	-2.7			
0011011	1Bh	-1.35	0110111	37h	-2.75			

Restriction

8.2.24 R83H (PTL): Partial Window Register

R83H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1st Parameter	W	1	-	-	-	PTH_ENB	-	-	HRST[9]	HRST[8]	00h
2nd Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	-	-	00h
3rd Parameter	W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4th Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	-	-	00h
5th Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
6th Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
7th Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
8th Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
9th Parameter	W	1	-	-	-	-	-	-	-	PMODE	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-This command sets partial window.

Name	Description
HRST[9:2]	Horizontal start address
HRED[9:2]	Horizontal end address. HRED must be greater than HRST.
VRST[9:0]	Vertical start address.
VRED[9:0]	Vertical end address. VRED must be greater than VRST.
PMODE	0: disable partial mode(default) 1: enable partial mode
PTH_ENB	0:Source output enable follow HRST and HRED 1:Source output disable

Note:
No matter HRST[1:0] ,HRST[9:8],HRED[9:8],VRST[9:8],VRED[9:8] value being filled, it's always be 00b.
No matter HRED[1:0] value being filled, it's always be 11b.

Gates scan both inside and outside of the partial window.

Note :No matter PTH_ENB setting , master/slave need define partial window

Restriction

8.2.25 R90H (PGM): Program Mode

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	0	1	0	0	0	0	90H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	

8.2.26 R91H (APG): Active Program

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	0	1	0	0	0	1	91H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

8.2.27 R92H (RMTP): Read MTP Data

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMTP	W	0	1	0	0	1	0	0	1	0	92H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x000 in the MTP								-
3rd Parameter	R	1	The data of address 0x001 in the MTP								-
4th Parameter	R	1	:								-
5th Parameter	R	1	The data of address (n-1) in the MTP								-
6th~(m-1)th Parameter	R	1	…..								-
mth Parameter	R	1	The data of address (n) in the MTP								-

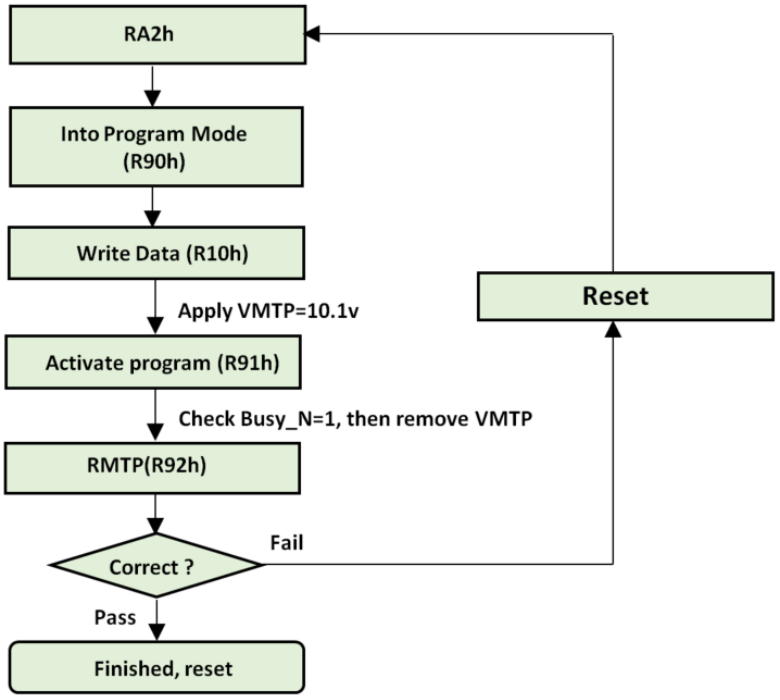
NOTE: "-" Don't care, can be set to VDD or GND level

Description

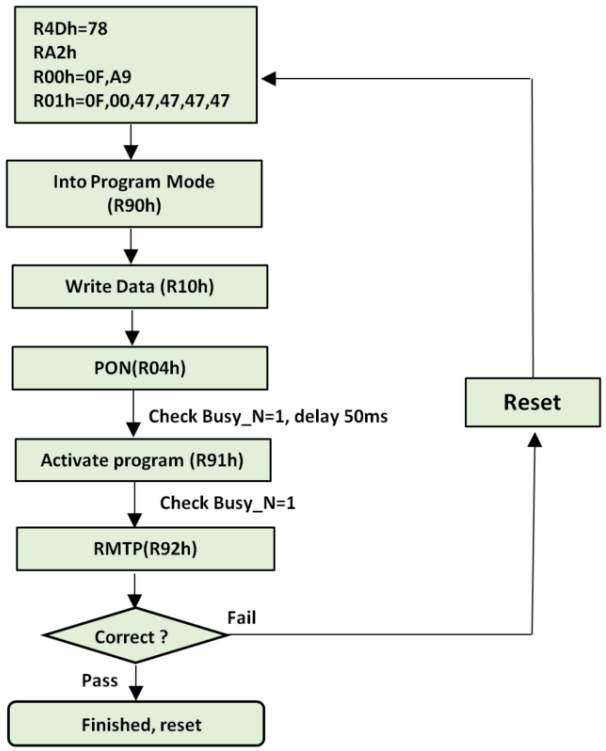
-The command define as follows:

The command is used for reading the content of MTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF



The sequence of programming MTP(External power)

	 The sequence of programming MTP(Internal power)
Restriction	This command only actives when BUSY_N = “1”.

8.2.28 RA2 (PGM_CFG): MTP Program Config Register (E Ink use only)

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM_CFG	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	W	1	-	-	-	VMTPSEL	-	-	M_dis	S_dis	00h
2nd Parameter	W	1	PGM_SADDR[15:8]								00h
3rd Parameter	W	1	PGM_SADDR[7:0]								00h
4th Parameter	W	1	PGM_DSIZE[15:8]								0Fh
5th Parameter	W	1	PGM_DSIZE[7:0]								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is used for setting configuration of MTP

1st Parameter:

Bit	Name	Description
0	S_dis	0: slave enable some command (default) 1: slave disable some command
1	M_dis	0: master enable some command (default) 1: master disable some command
4	VMTPSEL	0:External VMTP (default) 1:Internal VMTP

Bit[0] enable/disable some command when IC sets slave (MS pin is low)
Bit[1] enable/disable some command when IC sets master (MS pin is high)

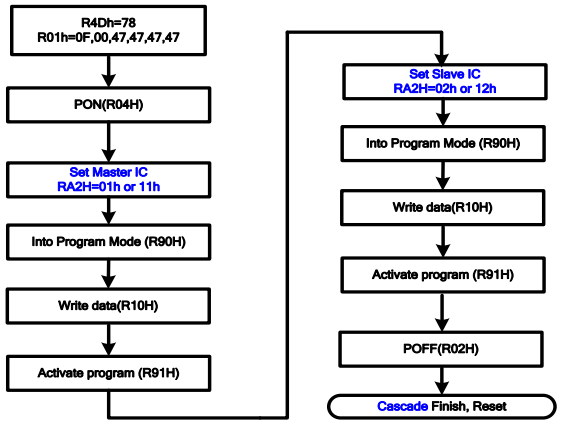
Note:
Some command define: R00H(Parameter 1) (PSR), R10H(DTM), R90H(PGM), R91H(APG), R83H(PTLW)

Command read

M_dis	S_dis	Description
0	0	command read from master
0	1	command read from master
1	0	command read from slave
1	1	command read from slave

2nd & 3rd Parameters: Program and Read MTP start address PGM_SADDR[15:0]
4th & 5th Parameters: Program data size PGM_DSIZE[15:0]

Note:
If user program Area0 (0x00~0x017F), PGM_SADDR[15:0] will be set 0x0000, PGM_DSIZE[15:0] will be set 0x0180.

	Cascade MTP Flow 
Restriction	

8.2.29 RE0H (CCSET): Cascade Setting (E Ink use only)

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

<table>
<tr><td>Description</td><td>This command is used for cascade.

1st Parameter:
<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0</td><td>CCEIN</td><td>Output clock enable/disable.
0: for single mode. (default)
1: for cascade mode.</td></tr>
<tr><td>1</td><td>TSFIX</td><td>Let the value of slave's temperature is same as the master's.
0: Temperature value is defined by internal temperature sensor/external LM75. (default)
1: Temperature value is defined by TS_SET [7:0] registers.</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

8.2.30 RE3H (PWS): Power Saving Register

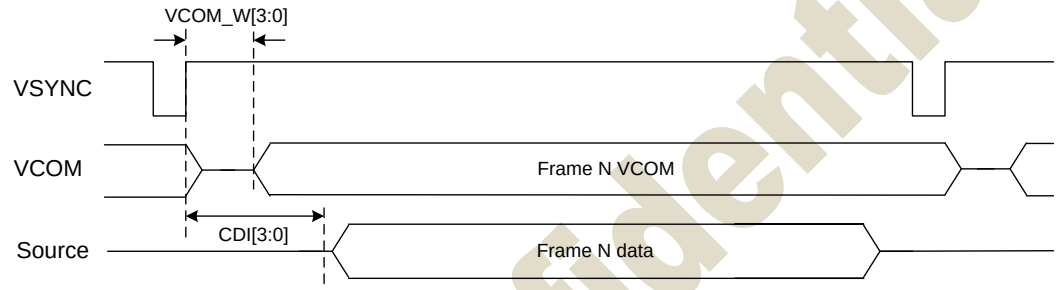
RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h

NOTE: "-" Don't care, can be set to VDD or GND level

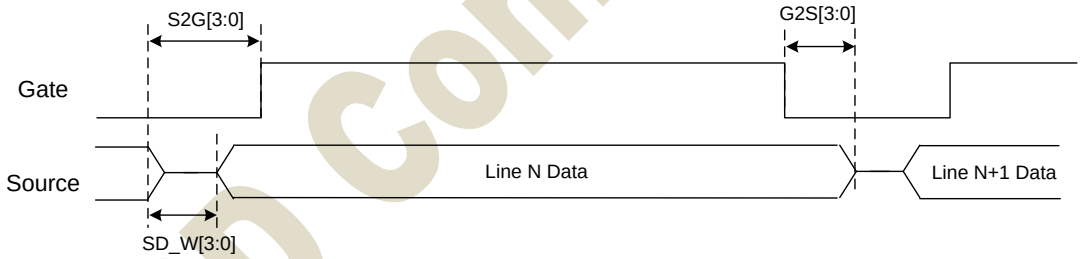
Description

- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W: VCOM power saving width (unit = line period)



SD_W: Source power saving width (unit = 500nS), SD_W<=S2G



Restriction

8.2.31 RE4H (LVSEL): LVD Voltage Select Register

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	LVD_SEL[1:0]: Low Power Voltage Selection
Restriction	

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

8.2.32 RE5H (CCS_SEL): Cascade Setting Select

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCS_sel	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	-	-	-	-	cascade_ sync	-	-	-	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used for cascade. 1st Parameter:

Bit	Name	Description
3	cascade_sync	0: cascade mode: sync_C / TSCL / TSDA (default) 1: cascade mode: sync_C / sync_D / sync_E

Restriction	

8.2.33 Register Restriction

Following table will indicate the register restriction:

Register	Refresh Restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R04H(PON)	X	Flag
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R17H(AUTO)	Valid in standby	Flag
R30H(PLL)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R61H(TRES)	X	No action
R65H(GSST)	X	No action
R70H(REV)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
R83H(PTL)	X	No action
R90H(PGM)	X	No action
R91H(APG)	X	Flag
R92H(RMTP)	X	Flag
RA2H(PGM_CFG)	X	No action
RE0H(CCSET)	X	No action
RE3H(PWS)	X	No action
RE4H(LVSEL)	X	No action
RE5H(CCS_SEL)	X	No action

9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

In order to prevent IC fail in power on resetting, the power sequence must be followed as below.

Power on Sequence

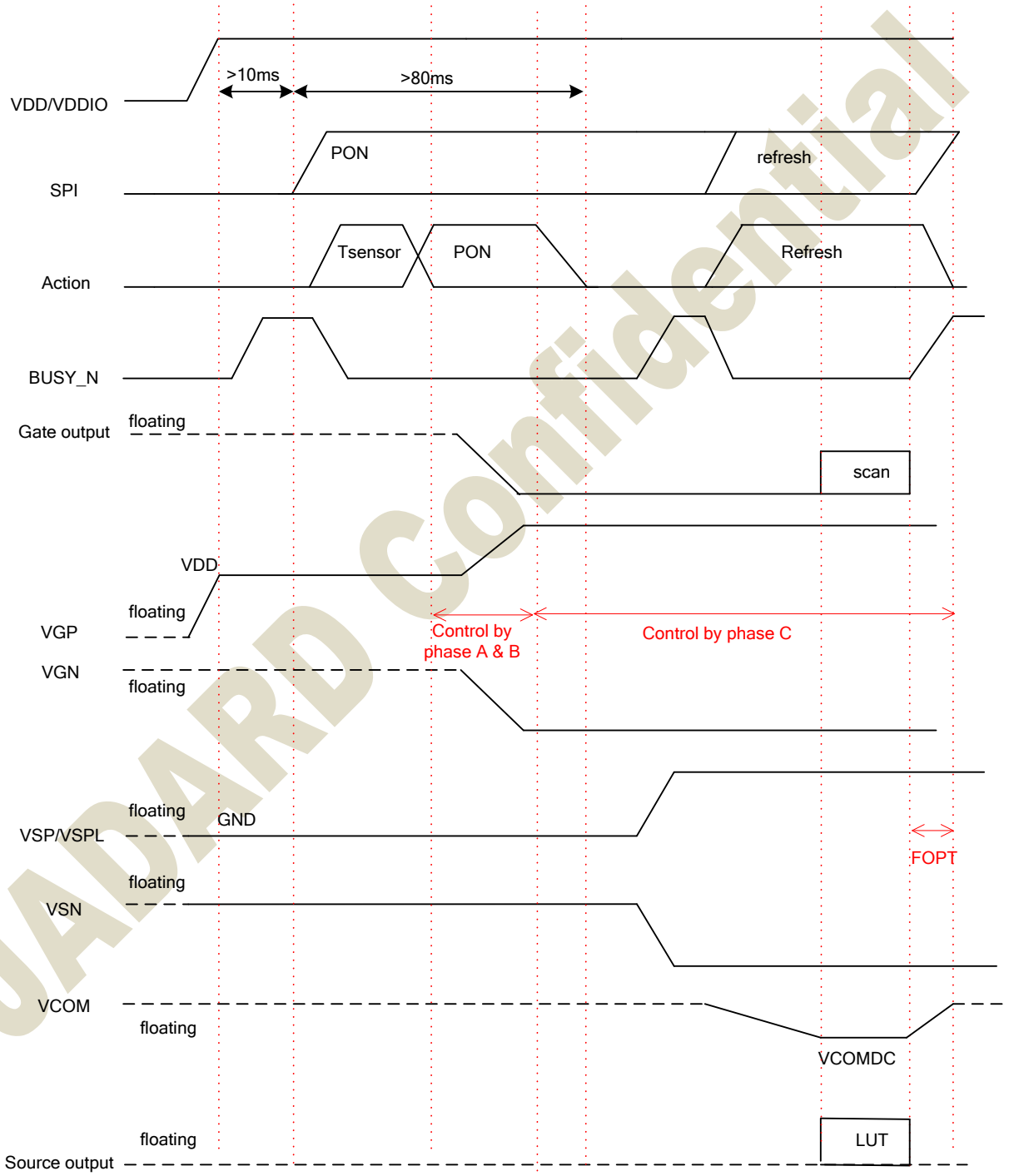


Figure 1: Power on sequence

Power off Sequence

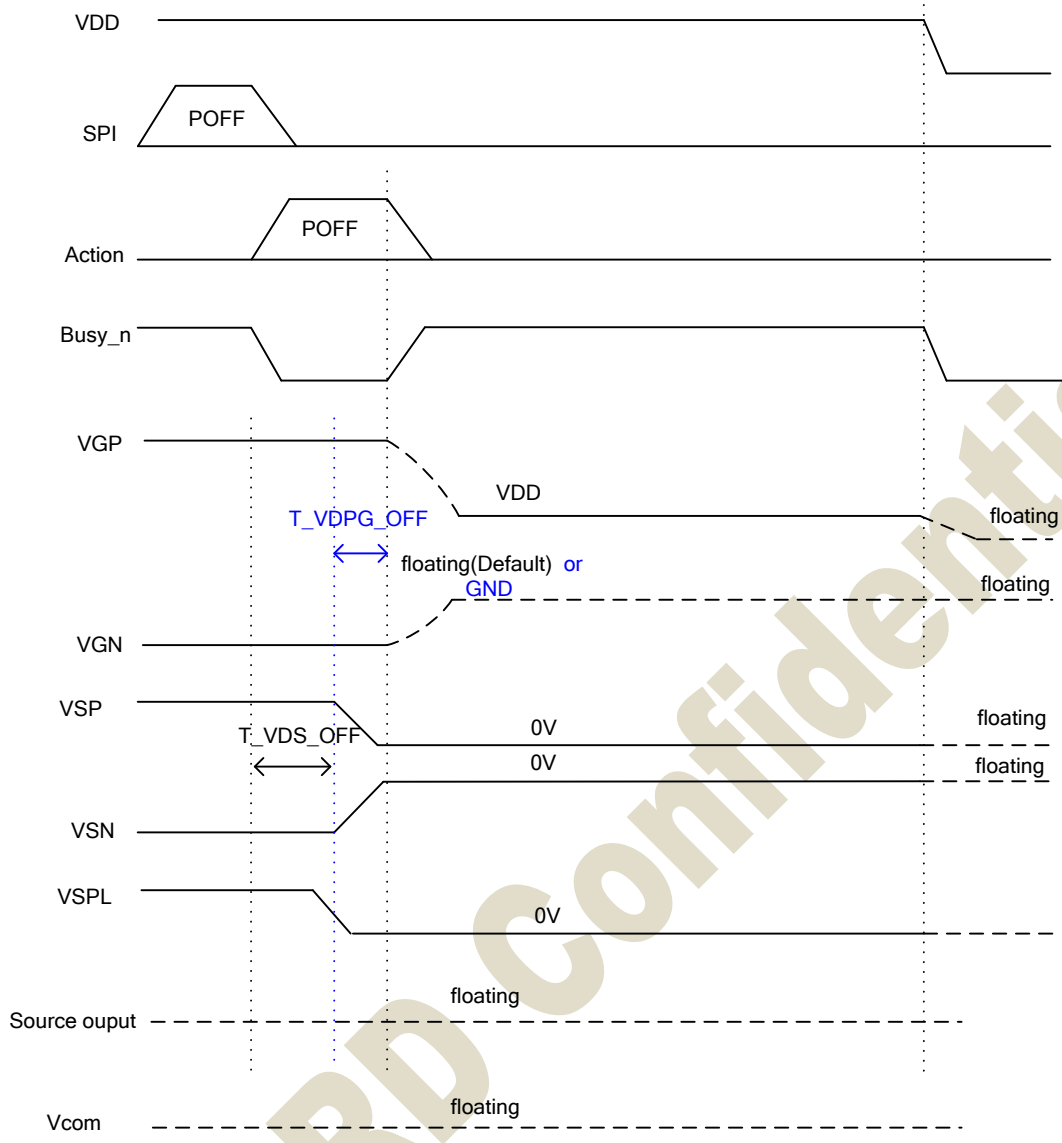


Figure 2: Power off sequence

DSLP sequence

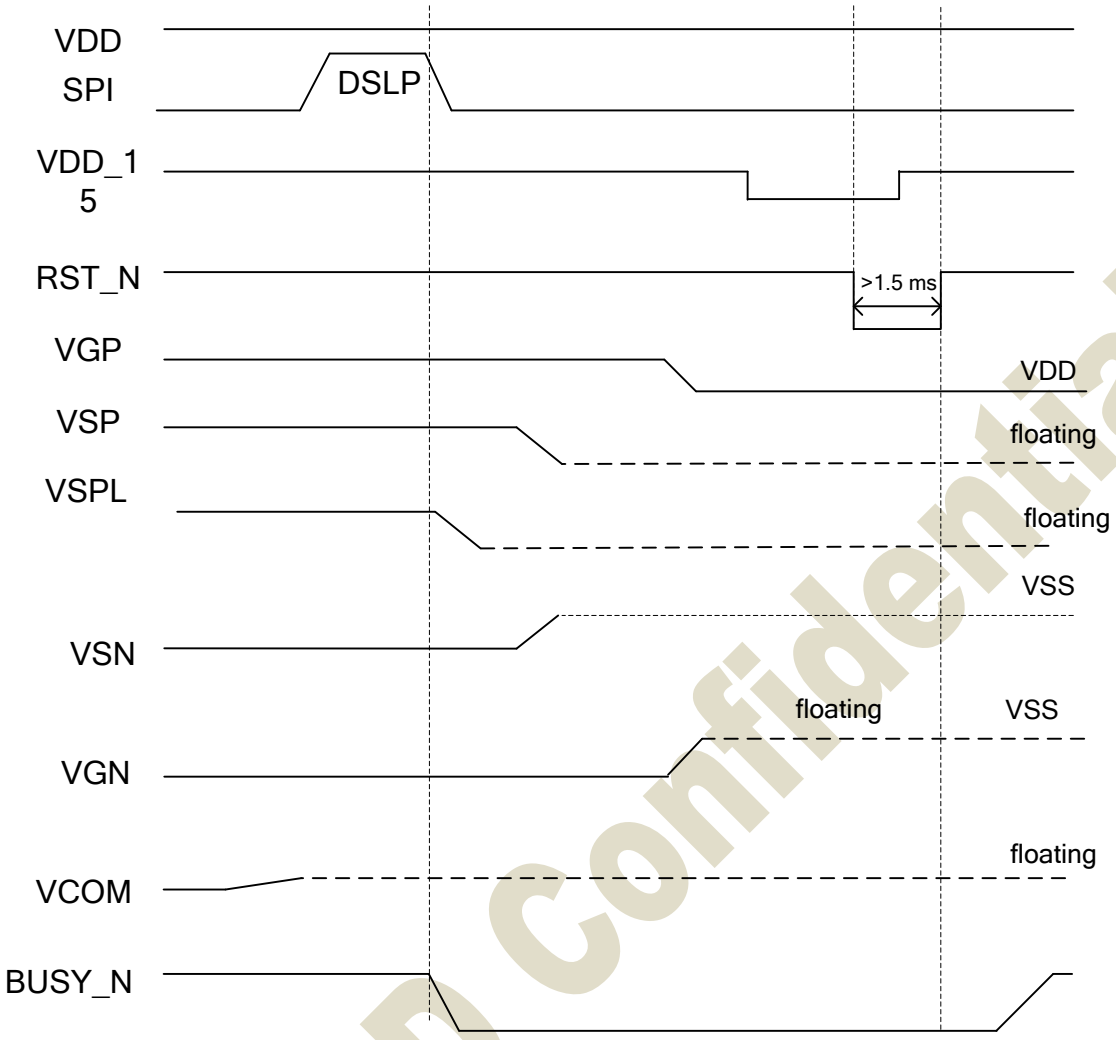


Figure 3: DSLP sequence

9.2 MTP LUT Definition

The MTP size would be 4096Bytes.

MTP bank 0 (4K bytes)	
Address(Hex)	Content
0x000~0xEFF	LUT compress data
0xF00~0xF58	Reserved
0xF59~0xF84	Default setting (44bytes)
0xF85~0xFFF	JD setting (123bytes)

9.3 Default Setting Format in MTP

	Addr. (Dec)	Addr. (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value (Hex)
	-	-	User Reserved bytes								00
--	3929	F59	Enable MTP Setting (0xA5)								A5
R85H	3930	F5A	Reserved								-
	3931	F5B	Reserved								-
R00H	3932	F5C	RES[1:0]		PST_MODE	-	UD	SHL	SHD_N	RST_N	0F
	3933	F5D	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09
R01H	3934	F5E	-	-	-	-	-	VSC_EN	VDS_EN	VDG_EN	07
	3935	F5F	-	-	-		-	-	VGP[1:0]		00
	3936	F60	-	VSPL_0[6:0]							00
	3937	F61	-	VSP_1[6:0]							00
	3938	F62	-	VSN_1[6:0]							00
	3939	F63	-	VSPL_1[6:0]							00
-	3940	F64	Reserved								00
	3941	F65	Reserved								00
	3942	F66	Reserved								54
	3943	F67	Reserved								44
R06H	3944	F68	-	-	-	-	PHB_SFT[1:0]		PHA_SFT[1:0]		00
	3945	F69	-	-	PHA_ON[5:0]						06
	3946	F6A	-	-	PHA_OFF[5:0]						02
	3947	F6B	-	-	PHB_ON[5:0]						07
	3948	F6C	-	-	PHB_OFF[5:0]						02
	3949	F6D	-	-	PHC_ON[5:0]						07
	3950	F6E	-	-	PHC_OFF[5:0]						02
-	3951	F6F	Reserved								00
R30H	3952	F70	-	-	-	-	Dyna	FR[2:0]			02
R50h	3953	F71	VBD[2:0]			DDX	CDI[3:0]				97
-	3954	F72	Reserved								02
	3955	F73	Reserved								02
R61H	3956	F74	-	-	-	-	-	-	HRES[9]	HRES[8]	00
	3957	F75	HRES[7:2]						0	0	00
	3958	F76	-	-	-	-	-	-	VRES[9]	VRES[8]	00
	3959	F77	VRES[7:0]								00
R65H	3960	F78	-	-	-	-	-	-	S_start(9)	S_start(8)	00
	3961	F79	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00
	3962	F7A	-	-	-	-	-	-	G_start(9)	G_start(8)	00
	3963	F7B	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00
R82H	3964	F7C		VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00
RE5H	3965	F7D	-	-	-	-	cascade_sync	-	-	-	00
R41H	3966	F7E	-	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00
RE0H	3967	F7F	-	-	-	-	-	-	TSFIX	CCEIN	00
RE3H	3968	F80	VCOM_W[3:0]				SD_W[3:0]				00
RE4H	3969	F81	-	-	-	-	-		LVD_SEL[1:0]		03
-	3970	F82	Reserved								03
	3971	F83	Reserved								1C
	3972	F84	Reserved								00
--	3973-4095	F85-FFF	JD setting								FF

9.1 Data transmission waveform

Example1: The driver will scan 1 frame to GND after waveform finished.(FOPT=0)

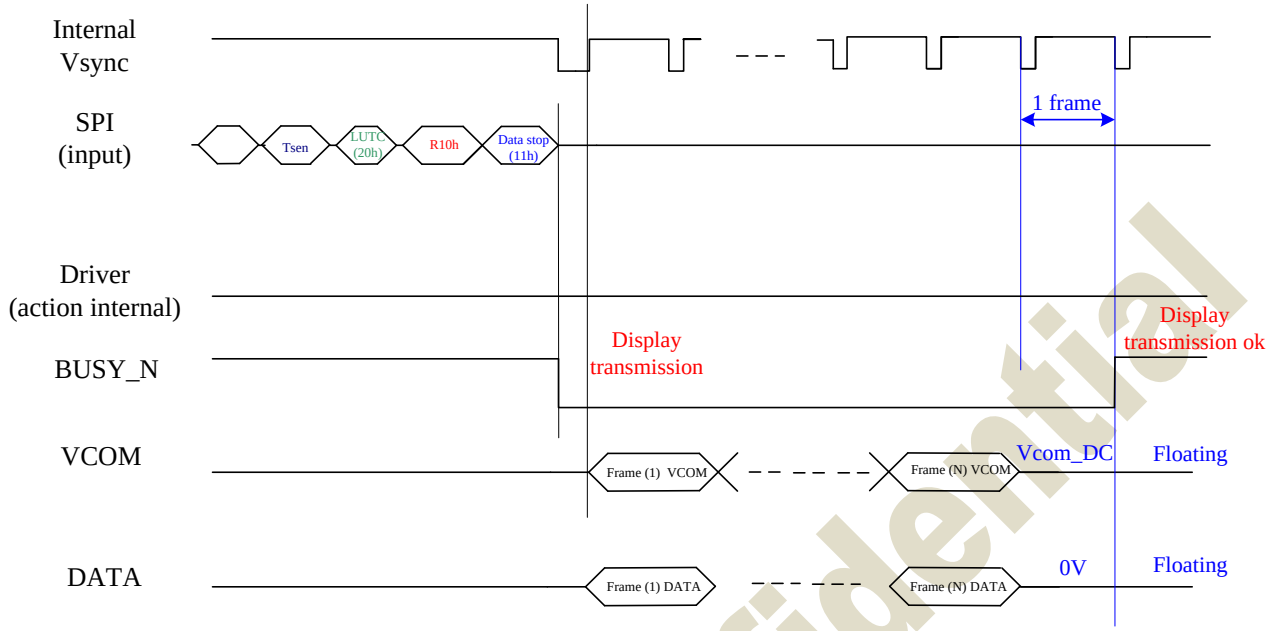


Figure 1: Data transmission example1 waveform

Example2: The driver will float VCOM and keep previous output data(FOPT=1)

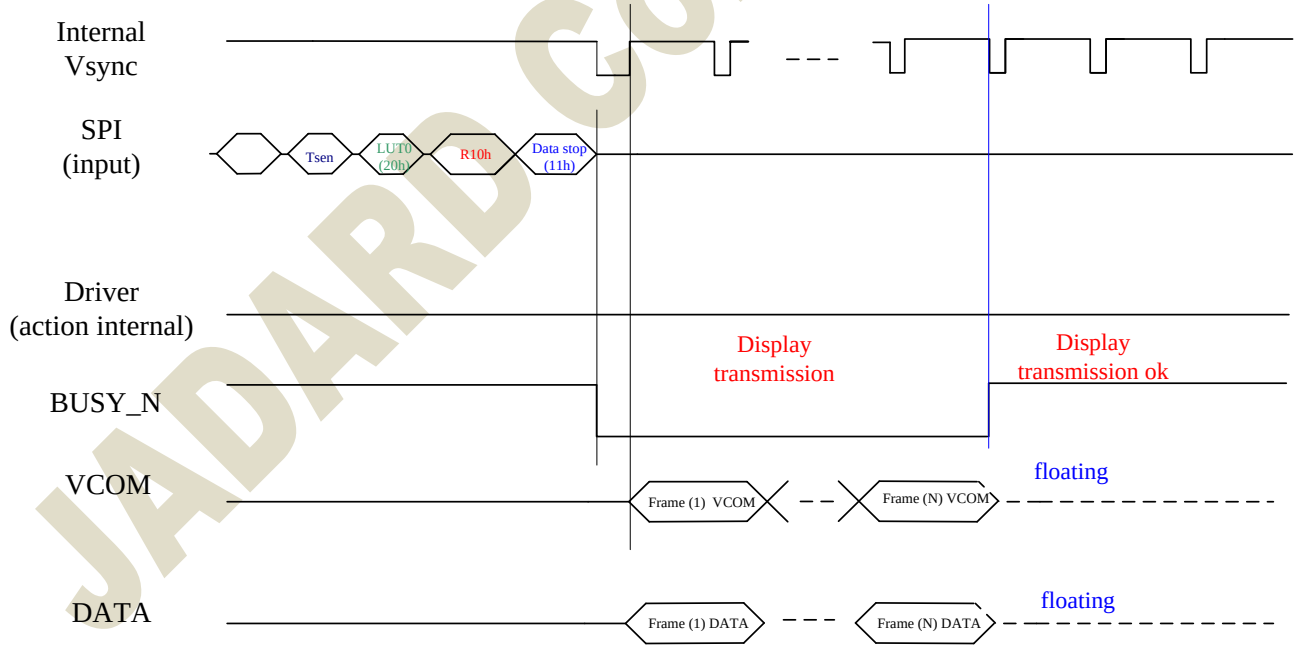


Figure 2: Display refresh example2 waveform

10. ELECTRICAL SPECIFICATIONS

10.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	VDDIO+0.3	V
Supply range	VGP-VGN	VGN-0.3	VGP+0.3	V
Analog supply	VSP_0	+15	+15	V
Analog supply	VSN_0	-15	-15	V
Analog supply	VSPL_0	+3	+15	V
Analog supply	VSP_1	+3	+15	V
Analog supply	VSN_1	-3	-15	V
Analog supply	VSPL_1	+3	+15	V
Supply voltage	VGP	+10	+20	V
Supply voltage	VGN	-20	-10	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

10.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.5V output voltage	VDD_15	1.35	1.5	1.65		
1.5V input voltage	VDD_15	1.35	1.5	1.65		
MTP program power	VMTP	9.8	10.1	10.2		
Digital ground	VSS		0			
DCDC ground	VSSP		0			
Low Level Input Voltage	Vil	GND	-	0.3Xvdd	V	Digital input pins
High Level Input Voltage	Vih	0.7Xvio	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400Ma
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400Ma DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL = -400Ma
Input Leakage Current	Iin	-1.0	-	+1.0	Ua	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Digital Stand-by Current (power off mode)	IstVDD*	-	0	1	Ua	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	Ma	
IO Stand-by Current (power off mode)	IstVDDIO*	-	0.4	1.0	Ua	All stopped
IO Operating Current	IVDDIO*	-	-	0.2	Ma	No load
Operating Current	IVDD1*	-	-	TBD	Ma	
Operating temperature	T_{op}	-30	-	85	℃	

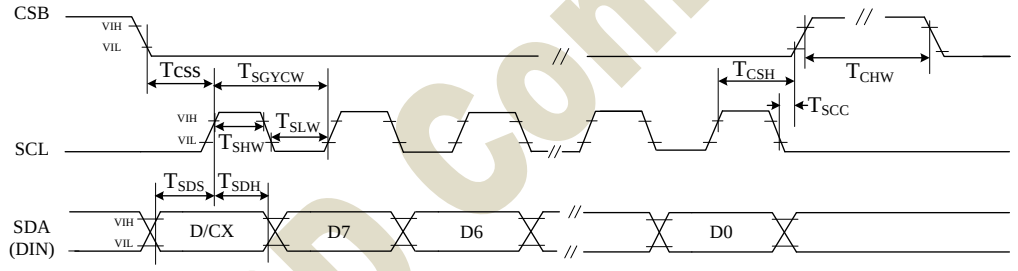
NOTE: typ. And max. values to be confirmed by design

10.3 Analog DC Characteristics

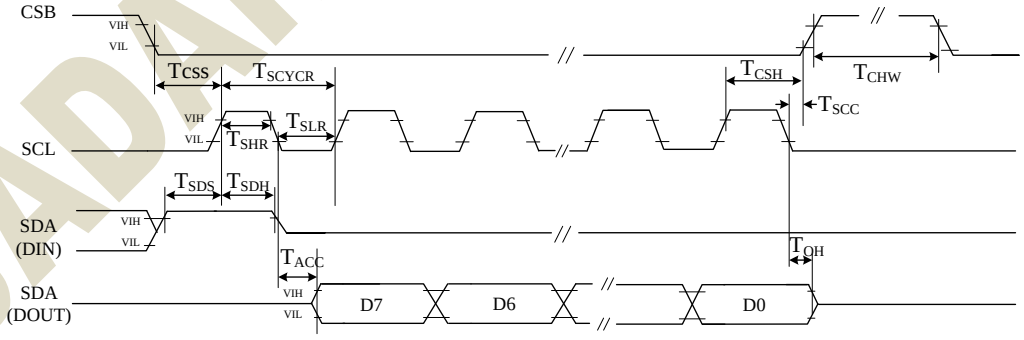
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSP	-	15	-	V	For source driver/VCOM
Positive Source voltage dev	Dvsp	-100	0	+100	Mv	
Negative Source voltage	VSn	-	-15	-	V	For source driver/VCOM
Negative Source voltage dev	Dvsn	-100	-	+100	Mv	
Positive Source voltage	VSPL_0	3		15		
Positive Source voltage dev.	Dvspl_0	-100	-	+100	Mv	
Positive Source voltage	VSP_1	3		15		
Positive Source voltage dev.	Dvsp_1	-100	-	+100	Mv	
Positive Source voltage	VSPL_1	3		15		
Positive Source voltage dev.	Dvspl_1	-100	-	+100	Mv	
VCOM voltage dev.	Dvcom	-200	-	+200	Mv	
Positive gate voltage dev	Dvgp	-500	-	+500	Mv	
Dynamic Range of Output	Vdr	0.1	-	VSP-0.1	V	
Voltage Range of VGP – VGN	VGP-VGN	-	-	41	V	
Negative Gate voltage	VGN	-10	-	-20	V	For gate driver
Positive Gate voltage	VGP	10		20	V	For gate driver
Positive HV Stand-by Current (power off mode)	IstVGP*	-	0	0.2	Ua	Include VSP power With load
Positive HV Operating Current	IVGP*	-	0.7	1.1	Ma	Include VSP power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVGP*	-	0.8	1.2	Ma	Include VSP power With load all SD=H VCOM external resistor divider not Included
Negative HV Stand-by Current (power off mode)	IstVGN*	-	0	0.2	Ma	Include VSP power With load
Negative HV Operating Current	IVGN*	-	0.8	1.2	Ma	Include VSN power With load all SD=L
Negative HV Operating Current	IVGN*	-	0.9-	1.3	Ma	Include VSN power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*	-	0	0.01	Ma	
VINT1 Operating Current	IVINT1*	-	-	0.3	Ma	
Voltage	IVINT1*	-	-	0.3	Ma	

10.4 AC Characteristics

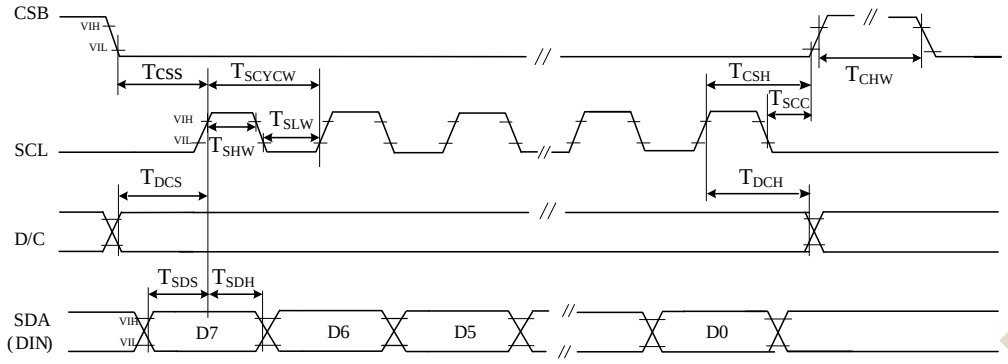
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T_{CSS}	60			ns	Chip select setup time
	T_{CSH}	65			ns	Chip select hold time
	T_{SCC}	20			ns	Chip select CSB setup time
	T_{CHW}	40			ns	Chip select setup time
SCL	T_{SCYCW}	100			ns	Serial clock cycle (Write)
	T_{SHW}	35			ns	SCL “H” pulse width (Write)
	T_{SLW}	35			ns	SCL “L” pulse width (Write)
	T_{SCYCR}	250			ns	Serial clock cycle (Read)
	T_{SHR}	60			ns	SCL “H” pulse width (Read)
	T_{SLR}	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	T_{SDS}	30			ns	Data setup time
	T_{SDH}	30			ns	Data hold time
	T_{ACC}			50	ns	Access time
	T_{OH}	15			ns	Output disable time
D/C	T_{DCS}	20			ns	DC setup time
	T_{DCH}	20			ns	DC hold time



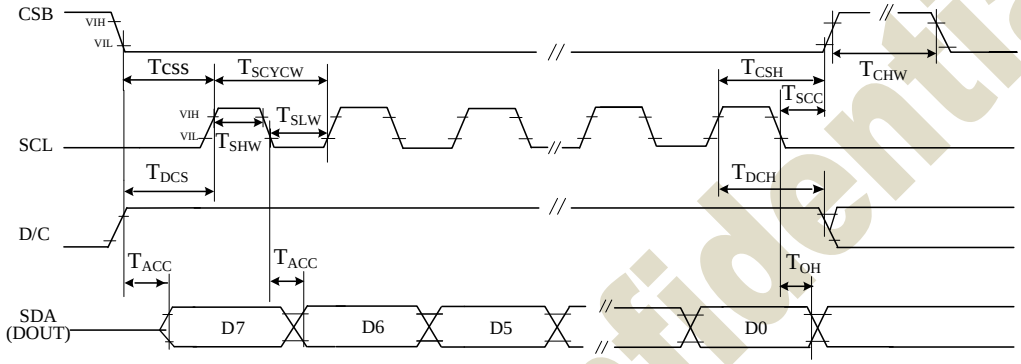
3 pin serial interface characteristics (write mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics(write mode)



4 pin serial interface characteristics(read mode)

Figure 9: SPI interface timing

11. CHIP OUTLINE DIMENSIONS

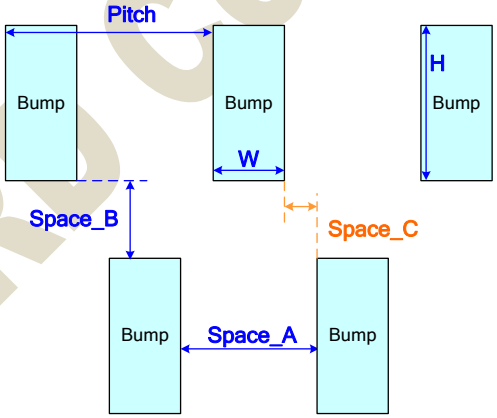
11.1 Circuit/Bump View

G1 G3 G5 ...G249 S127 ~ S0 G248... G4 G2 G0

JD79676
(face up)

Die Size:**7586um * 846um** (including scribe line 60um)
Die Size:**7526um * 786um**
Die Thickness:230 μm ± 20μm
Die TTV:(D_{MAX} – D_{MIN}) within die ≤ 2μm
Bump Height:9 μm ± 2μm
(H_{MAX} – H_{MIN}) within die ≤ 2μm
Hardness: 75 Hv ±25Hv
Coordinate origin:Chip center

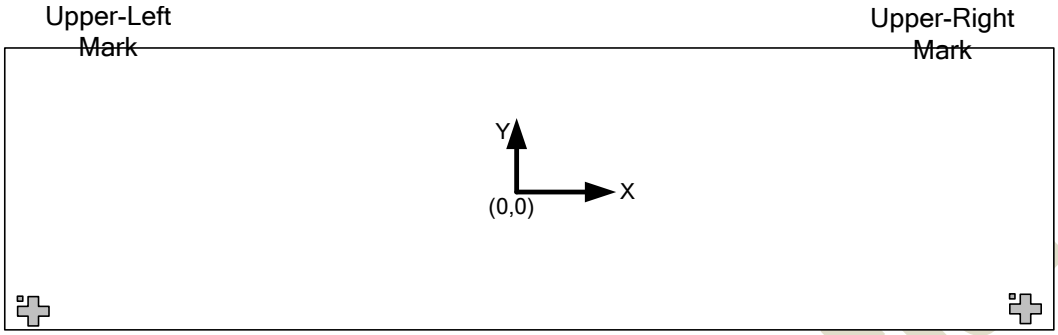
11.2 Bump information



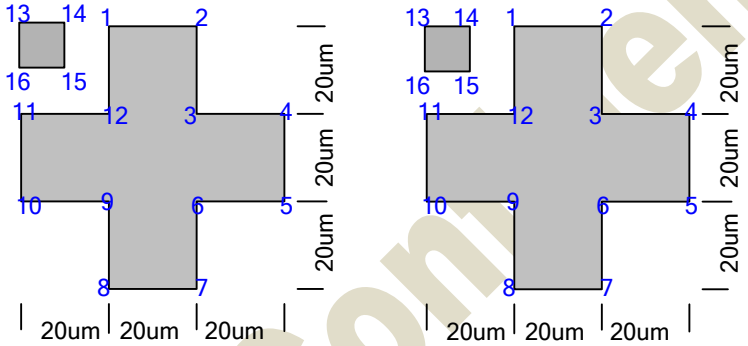
Bump type	Pitch	Space_A	Space_B	Space_C	W	H	area(um2)	Q'ty	Total area(um2)	
Input PAD	46	15	-	-	31	63	1953	155	302715	
Source PAD	26	14	19	1	12	89	1068	132	140976	717687
Gate PAD	42	24	19	3	18	59	1062	258	273996	

12. ALIGNMENT MARK INFORMATION

12.1 Location



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-3627	-327	3627	-327
1	-3637	-297	3617	-297
2	-3617	-297	3637	-297
3	-3617	-317	3637	-317
4	-3597	-317	3657	-317
5	-3597	-337	3657	-337
6	-3617	-337	3637	-337
7	-3617	-357	3637	-357
8	-3637	-357	3617	-357
9	-3637	-337	3617	-337
10	-3657	-337	3597	-337
11	-3657	-317	3597	-317
12	-3637	-317	3617	-317
13	-3657	-297	3597	-297
14	-3647	-297	3607	-297
15	-3647	-307	3607	-307
16	-3657	-307	3597	-307

12.2 Pad coordinates

No.	Name	X-axis	Y-axis	W	H
1	T_EN_LSH	-3542	-327.5	31	63
2	VGN	-3496	-327.5	31	63
3	VGN	-3450	-327.5	31	63
4	VGN	-3404	-327.5	31	63
5	VGN	-3358	-327.5	31	63
6	VGN	-3312	-327.5	31	63
7	VGN	-3266	-327.5	31	63
8	VGN	-3220	-327.5	31	63
9	VGN	-3174	-327.5	31	63
10	VGN	-3128	-327.5	31	63
11	VGN	-3082	-327.5	31	63
12	VGN	-3036	-327.5	31	63
13	VSSA	-2990	-327.5	31	63
14	VSN	-2944	-327.5	31	63
15	VSN	-2898	-327.5	31	63
16	VSN	-2852	-327.5	31	63
17	VSN	-2806	-327.5	31	63
18	VSN	-2760	-327.5	31	63
19	VSN	-2714	-327.5	31	63
20	VSN	-2668	-327.5	31	63
21	VSSA	-2622	-327.5	31	63
22	VGP	-2576	-327.5	31	63
23	VGP	-2530	-327.5	31	63
24	VGP	-2484	-327.5	31	63
25	VGP	-2438	-327.5	31	63
26	VGP	-2392	-327.5	31	63
27	VGP	-2346	-327.5	31	63
28	VSSA	-2300	-327.5	31	63
29	VSP	-2254	-327.5	31	63
30	VSP	-2208	-327.5	31	63
31	VSP	-2162	-327.5	31	63
32	VSP	-2116	-327.5	31	63
33	VSP	-2070	-327.5	31	63
34	VSP	-2024	-327.5	31	63
35	VSSA	-1978	-327.5	31	63
36	VMTP	-1932	-327.5	31	63
37	VMTP	-1886	-327.5	31	63
38	VMTP	-1840	-327.5	31	63
39	VDD_15V	-1794	-327.5	31	63
40	VDD_15V	-1748	-327.5	31	63
41	VDD_15V	-1702	-327.5	31	63
42	VDD_15V	-1656	-327.5	31	63
43	VDD_15V	-1610	-327.5	31	63
44	VDD_15V	-1564	-327.5	31	63
45	VSSA	-1518	-327.5	31	63
46	VSSA	-1472	-327.5	31	63
47	VSSA	-1426	-327.5	31	63
48	VSSA	-1380	-327.5	31	63
49	VSSA	-1334	-327.5	31	63
50	VSSA	-1288	-327.5	31	63
51	VSSA	-1242	-327.5	31	63
52	VSSA	-1196	-327.5	31	63
53	VSS	-1150	-327.5	31	63
54	VSS	-1104	-327.5	31	63
55	VSS	-1058	-327.5	31	63
56	VSS	-1012	-327.5	31	63
57	VSS	-966	-327.5	31	63
58	VSS	-920	-327.5	31	63

No.	Name	X-axis	Y-axis	W	H
59	VSS	-874	-327.5	31	63
60	VSS	-828	-327.5	31	63
61	VDDP	-782	-327.5	31	63
62	VDDP	-736	-327.5	31	63
63	VDDP	-690	-327.5	31	63
64	VDDP	-644	-327.5	31	63
65	VDDP	-598	-327.5	31	63
66	VDDP	-552	-327.5	31	63
67	VDDP	-506	-327.5	31	63
68	VDDP	-460	-327.5	31	63
69	VDD	-414	-327.5	31	63
70	VDD	-368	-327.5	31	63
71	VDD	-322	-327.5	31	63
72	VDD	-276	-327.5	31	63
73	VDD	-230	-327.5	31	63
74	VDD	-184	-327.5	31	63
75	VDD	-138	-327.5	31	63
76	T_VREF	-92	-327.5	31	63
77	T_VTSEN	-46	-327.5	31	63
78	T_SAR_REF	0	-327.5	31	63
79	SYNCE	46	-327.5	31	63
80	T_DEBUG[8]	92	-327.5	31	63
81	T_IN[2]	138	-327.5	31	63
82	T_DEBUG[7]	184	-327.5	31	63
83	T_DEBUG[6]	230	-327.5	31	63
84	T_EN_DIG	276	-327.5	31	63
85	VDDIO	322	-327.5	31	63
86	VDDIO	368	-327.5	31	63
87	VDDIO	414	-327.5	31	63
88	VDDIO	460	-327.5	31	63
89	T_IBIAS	506	-327.5	31	63
90	SDA	552	-327.5	31	63
91	SCL	598	-327.5	31	63
92	VSS	644	-327.5	31	63
93	CSB	690	-327.5	31	63
94	VDDIO	736	-327.5	31	63
95	T_DEBUG[5]	782	-327.5	31	63
96	T_IN[1]	828	-327.5	31	63
97	DC	874	-327.5	31	63
98	VDDIO	920	-327.5	31	63
99	T_DEBUG[4]	966	-327.5	31	63
100	VSS	1012	-327.5	31	63
101	RST_N	1058	-327.5	31	63
102	BUSY_N	1104	-327.5	31	63
103	SYNCC	1150	-327.5	31	63
104	VDDIO	1196	-327.5	31	63
105	T_DEBUG[3]	1242	-327.5	31	63
106	T_EX_REFCLK	1288	-327.5	31	63
107	T_DEBUG[2]	1334	-327.5	31	63
108	VDDIO	1380	-327.5	31	63
109	BS	1426	-327.5	31	63
110	T_IN[0]	1472	-327.5	31	63
111	T_DEBUG[1]	1518	-327.5	31	63
112	VDDIO	1564	-327.5	31	63
113	PCKI	1610	-327.5	31	63
114	T_EX_SYSCLK	1656	-327.5	31	63
115	MS	1702	-327.5	31	63
116	VDDIO	1748	-327.5	31	63

No.	Name	X-axis	Y-axis	W	H
117	TSDA	1794	-327.5	31	63
118	TSDA	1840	-327.5	31	63
119	TSCL	1886	-327.5	31	63
120	TSCL	1932	-327.5	31	63
121	PCKO	1978	-327.5	31	63
122	SYNCD	2024	-327.5	31	63
123	VSS	2070	-327.5	31	63
124	T_DEBUG[0]	2116	-327.5	31	63
125	VSPL	2162	-327.5	31	63
126	VSPL	2208	-327.5	31	63
127	VSPL	2254	-327.5	31	63
128	VSPL	2300	-327.5	31	63
129	VSPL	2346	-327.5	31	63
130	VSPL	2392	-327.5	31	63
131	VSSA	2438	-327.5	31	63
132	FB	2484	-327.5	31	63
133	FB	2530	-327.5	31	63
134	VSSA	2576	-327.5	31	63
135	RESE	2622	-327.5	31	63
136	RESE	2668	-327.5	31	63
137	VSSA	2714	-327.5	31	63
138	GDR	2760	-327.5	31	63
139	GDR	2806	-327.5	31	63
140	GDR	2852	-327.5	31	63
141	GDR	2898	-327.5	31	63
142	GDR	2944	-327.5	31	63
143	GDR	2990	-327.5	31	63
144	VSSA	3036	-327.5	31	63
145	VSSA	3082	-327.5	31	63
146	VCOM	3128	-327.5	31	63
147	VCOM	3174	-327.5	31	63
148	VCOM	3220	-327.5	31	63
149	VCOM	3266	-327.5	31	63
150	VCOM	3312	-327.5	31	63
151	VCOM	3358	-327.5	31	63
152	VCOM	3404	-327.5	31	63
153	VCOM	3450	-327.5	31	63
154	VCOM	3496	-327.5	31	63
155	T_VCOM	3542	-327.5	31	63
156	T_LDON5V	3645	354.5	18	59
157	T_VSPD_REF	3624	276.5	18	59
158	G[0]	3603	354.5	18	59
159	G[2]	3582	276.5	18	59
160	G[4]	3561	354.5	18	59
161	G[6]	3540	276.5	18	59
162	G[8]	3519	354.5	18	59
163	G[10]	3498	276.5	18	59
164	G[12]	3477	354.5	18	59
165	G[14]	3456	276.5	18	59
166	G[16]	3435	354.5	18	59
167	G[18]	3414	276.5	18	59
168	G[20]	3393	354.5	18	59
169	G[22]	3372	276.5	18	59
170	G[24]	3351	354.5	18	59
171	G[26]	3330	276.5	18	59
172	G[28]	3309	354.5	18	59
173	G[30]	3288	276.5	18	59
174	G[32]	3267	354.5	18	59
175	G[34]	3246	276.5	18	59
176	G[36]	3225	354.5	18	59

No.	Name	X-axis	Y-axis	W	H
177	G[38]	3204	276.5	18	59
178	G[40]	3183	354.5	18	59
179	G[42]	3162	276.5	18	59
180	G[44]	3141	354.5	18	59
181	G[46]	3120	276.5	18	59
182	G[48]	3099	354.5	18	59
183	G[50]	3078	276.5	18	59
184	G[52]	3057	354.5	18	59
185	G[54]	3036	276.5	18	59
186	G[56]	3015	354.5	18	59
187	G[58]	2994	276.5	18	59
188	G[60]	2973	354.5	18	59
189	G[62]	2952	276.5	18	59
190	G[64]	2931	354.5	18	59
191	G[66]	2910	276.5	18	59
192	G[68]	2889	354.5	18	59
193	G[70]	2868	276.5	18	59
194	G[72]	2847	354.5	18	59
195	G[74]	2826	276.5	18	59
196	G[76]	2805	354.5	18	59
197	G[78]	2784	276.5	18	59
198	G[80]	2763	354.5	18	59
199	G[82]	2742	276.5	18	59
200	G[84]	2721	354.5	18	59
201	G[86]	2700	276.5	18	59
202	G[88]	2679	354.5	18	59
203	G[90]	2658	276.5	18	59
204	G[92]	2637	354.5	18	59
205	G[94]	2616	276.5	18	59
206	G[96]	2595	354.5	18	59
207	G[98]	2574	276.5	18	59
208	G[100]	2553	354.5	18	59
209	G[102]	2532	276.5	18	59
210	G[104]	2511	354.5	18	59
211	G[106]	2490	276.5	18	59
212	G[108]	2469	354.5	18	59
213	G[110]	2448	276.5	18	59
214	G[112]	2427	354.5	18	59
215	G[114]	2406	276.5	18	59
216	G[116]	2385	354.5	18	59
217	G[118]	2364	276.5	18	59
218	G[120]	2343	354.5	18	59
219	G[122]	2322	276.5	18	59
220	G[124]	2301	354.5	18	59
221	G[126]	2280	276.5	18	59
222	G[128]	2259	354.5	18	59
223	G[130]	2238	276.5	18	59
224	G[132]	2217	354.5	18	59
225	G[134]	2196	276.5	18	59
226	G[136]	2175	354.5	18	59
227	G[138]	2154	276.5	18	59
228	G[140]	2133	354.5	18	59
229	G[142]	2112	276.5	18	59
230	G[144]	2091	354.5	18	59
231	G[146]	2070	276.5	18	59
232	G[148]	2049	354.5	18	59
233	G[150]	2028	276.5	18	59
234	G[152]	2007	354.5	18	59
235	G[154]	1986	276.5	18	59
236	G[156]	1965	354.5	18	59

No.	Name	X-axis	Y-axis	W	H
237	G[158]	1944	276.5	18	59
238	G[160]	1923	354.5	18	59
239	G[162]	1902	276.5	18	59
240	G[164]	1881	354.5	18	59
241	G[166]	1860	276.5	18	59
242	G[168]	1839	354.5	18	59
243	G[170]	1818	276.5	18	59
244	G[172]	1797	354.5	18	59
245	G[174]	1776	276.5	18	59
246	G[176]	1755	354.5	18	59
247	G[178]	1734	276.5	18	59
248	G[180]	1713	354.5	18	59
249	G[182]	1692	276.5	18	59
250	G[184]	1671	354.5	18	59
251	G[186]	1650	276.5	18	59
252	G[188]	1629	354.5	18	59
253	G[190]	1608	276.5	18	59
254	G[192]	1587	354.5	18	59
255	G[194]	1566	276.5	18	59
256	G[196]	1545	354.5	18	59
257	G[198]	1524	276.5	18	59
258	G[200]	1503	354.5	18	59
259	G[202]	1482	276.5	18	59
260	G[204]	1461	354.5	18	59
261	G[206]	1440	276.5	18	59
262	G[208]	1419	354.5	18	59
263	G[210]	1398	276.5	18	59
264	G[212]	1377	354.5	18	59
265	G[214]	1356	276.5	18	59
266	G[216]	1335	354.5	18	59
267	G[218]	1314	276.5	18	59
268	G[220]	1293	354.5	18	59
269	G[222]	1272	276.5	18	59
270	G[224]	1251	354.5	18	59
271	G[226]	1230	276.5	18	59
272	G[228]	1209	354.5	18	59
273	G[230]	1188	276.5	18	59
274	G[232]	1167	354.5	18	59
275	G[234]	1146	276.5	18	59
276	G[236]	1125	354.5	18	59
277	G[238]	1104	276.5	18	59
278	G[240]	1083	354.5	18	59
279	G[242]	1062	276.5	18	59
280	G[244]	1041	354.5	18	59
281	G[246]	1020	276.5	18	59
282	G[248]	999	354.5	18	59
283	DUMMY[0]	978	276.5	18	59
284	DUMMY[1]	957	354.5	18	59
285	DUMMY[2]	851.5	339.5	12	89
286	VBD[1]	838.5	231.5	12	89
287	S[0]	825.5	339.5	12	89
288	S[1]	812.5	231.5	12	89
289	S[2]	799.5	339.5	12	89
290	S[3]	786.5	231.5	12	89
291	S[4]	773.5	339.5	12	89
292	S[5]	760.5	231.5	12	89
293	S[6]	747.5	339.5	12	89
294	S[7]	734.5	231.5	12	89
295	S[8]	721.5	339.5	12	89
296	S[9]	708.5	231.5	12	89

No.	Name	X-axis	Y-axis	W	H
297	S[10]	695.5	339.5	12	89
298	S[11]	682.5	231.5	12	89
299	S[12]	669.5	339.5	12	89
300	S[13]	656.5	231.5	12	89
301	S[14]	643.5	339.5	12	89
302	S[15]	630.5	231.5	12	89
303	S[16]	617.5	339.5	12	89
304	S[17]	604.5	231.5	12	89
305	S[18]	591.5	339.5	12	89
306	S[19]	578.5	231.5	12	89
307	S[20]	565.5	339.5	12	89
308	S[21]	552.5	231.5	12	89
309	S[22]	539.5	339.5	12	89
310	S[23]	526.5	231.5	12	89
311	S[24]	513.5	339.5	12	89
312	S[25]	500.5	231.5	12	89
313	S[26]	487.5	339.5	12	89
314	S[27]	474.5	231.5	12	89
315	S[28]	461.5	339.5	12	89
316	S[29]	448.5	231.5	12	89
317	S[30]	435.5	339.5	12	89
318	S[31]	422.5	231.5	12	89
319	S[32]	409.5	339.5	12	89
320	S[33]	396.5	231.5	12	89
321	S[34]	383.5	339.5	12	89
322	S[35]	370.5	231.5	12	89
323	S[36]	357.5	339.5	12	89
324	S[37]	344.5	231.5	12	89
325	S[38]	331.5	339.5	12	89
326	S[39]	318.5	231.5	12	89
327	S[40]	305.5	339.5	12	89
328	S[41]	292.5	231.5	12	89
329	S[42]	279.5	339.5	12	89
330	S[43]	266.5	231.5	12	89
331	S[44]	253.5	339.5	12	89
332	S[45]	240.5	231.5	12	89
333	S[46]	227.5	339.5	12	89
334	S[47]	214.5	231.5	12	89
335	S[48]	201.5	339.5	12	89
336	S[49]	188.5	231.5	12	89
337	S[50]	175.5	339.5	12	89
338	S[51]	162.5	231.5	12	89
339	S[52]	149.5	339.5	12	89
340	S[53]	136.5	231.5	12	89
341	S[54]	123.5	339.5	12	89
342	S[55]	110.5	231.5	12	89
343	S[56]	97.5	339.5	12	89
344	S[57]	84.5	231.5	12	89
345	S[58]	71.5	339.5	12	89
346	S[59]	58.5	231.5	12	89
347	S[60]	45.5	339.5	12	89
348	S[61]	32.5	231.5	12	89
349	S[62]	19.5	339.5	12	89
350	S[63]	6.5	231.5	12	89
351	S[64]	-6.5	339.5	12	89
352	S[65]	-19.5	231.5	12	89
353	S[66]	-32.5	339.5	12	89
354	S[67]	-45.5	231.5	12	89
355	S[68]	-58.5	339.5	12	89
356	S[69]	-71.5	231.5	12	89

No.	Name	X-axis	Y-axis	W	H
357	S[70]	-84.5	339.5	12	89
358	S[71]	-97.5	231.5	12	89
359	S[72]	-110.5	339.5	12	89
360	S[73]	-123.5	231.5	12	89
361	S[74]	-136.5	339.5	12	89
362	S[75]	-149.5	231.5	12	89
363	S[76]	-162.5	339.5	12	89
364	S[77]	-175.5	231.5	12	89
365	S[78]	-188.5	339.5	12	89
366	S[79]	-201.5	231.5	12	89
367	S[80]	-214.5	339.5	12	89
368	S[81]	-227.5	231.5	12	89
369	S[82]	-240.5	339.5	12	89
370	S[83]	-253.5	231.5	12	89
371	S[84]	-266.5	339.5	12	89
372	S[85]	-279.5	231.5	12	89
373	S[86]	-292.5	339.5	12	89
374	S[87]	-305.5	231.5	12	89
375	S[88]	-318.5	339.5	12	89
376	S[89]	-331.5	231.5	12	89
377	S[90]	-344.5	339.5	12	89
378	S[91]	-357.5	231.5	12	89
379	S[92]	-370.5	339.5	12	89
380	S[93]	-383.5	231.5	12	89
381	S[94]	-396.5	339.5	12	89
382	S[95]	-409.5	231.5	12	89
383	S[96]	-422.5	339.5	12	89
384	S[97]	-435.5	231.5	12	89
385	S[98]	-448.5	339.5	12	89
386	S[99]	-461.5	231.5	12	89
387	S[100]	-474.5	339.5	12	89
388	S[101]	-487.5	231.5	12	89
389	S[102]	-500.5	339.5	12	89
390	S[103]	-513.5	231.5	12	89
391	S[104]	-526.5	339.5	12	89
392	S[105]	-539.5	231.5	12	89
393	S[106]	-552.5	339.5	12	89
394	S[107]	-565.5	231.5	12	89
395	S[108]	-578.5	339.5	12	89
396	S[109]	-591.5	231.5	12	89
397	S[110]	-604.5	339.5	12	89
398	S[111]	-617.5	231.5	12	89
399	S[112]	-630.5	339.5	12	89
400	S[113]	-643.5	231.5	12	89
401	S[114]	-656.5	339.5	12	89
402	S[115]	-669.5	231.5	12	89
403	S[116]	-682.5	339.5	12	89
404	S[117]	-695.5	231.5	12	89
405	S[118]	-708.5	339.5	12	89
406	S[119]	-721.5	231.5	12	89
407	S[120]	-734.5	339.5	12	89
408	S[121]	-747.5	231.5	12	89
409	S[122]	-760.5	339.5	12	89
410	S[123]	-773.5	231.5	12	89
411	S[124]	-786.5	339.5	12	89
412	S[125]	-799.5	231.5	12	89
413	S[126]	-812.5	339.5	12	89
414	S[127]	-825.5	231.5	12	89
415	VBD[2]	-838.5	339.5	12	89
416	DUMMY[3]	-851.5	231.5	12	89

No.	Name	X-axis	Y-axis	W	H
417	DUMMY[4]	-957	354.5	18	59
418	DUMMY[5]	-978	276.5	18	59
419	G[249]	-999	354.5	18	59
420	G[247]	-1020	276.5	18	59
421	G[245]	-1041	354.5	18	59
422	G[243]	-1062	276.5	18	59
423	G[241]	-1083	354.5	18	59
424	G[239]	-1104	276.5	18	59
425	G[237]	-1125	354.5	18	59
426	G[235]	-1146	276.5	18	59
427	G[233]	-1167	354.5	18	59
428	G[231]	-1188	276.5	18	59
429	G[229]	-1209	354.5	18	59
430	G[227]	-1230	276.5	18	59
431	G[225]	-1251	354.5	18	59
432	G[223]	-1272	276.5	18	59
433	G[221]	-1293	354.5	18	59
434	G[219]	-1314	276.5	18	59
435	G[217]	-1335	354.5	18	59
436	G[215]	-1356	276.5	18	59
437	G[213]	-1377	354.5	18	59
438	G[211]	-1398	276.5	18	59
439	G[209]	-1419	354.5	18	59
440	G[207]	-1440	276.5	18	59
441	G[205]	-1461	354.5	18	59
442	G[203]	-1482	276.5	18	59
443	G[201]	-1503	354.5	18	59
444	G[199]	-1524	276.5	18	59
445	G[197]	-1545	354.5	18	59
446	G[195]	-1566	276.5	18	59
447	G[193]	-1587	354.5	18	59
448	G[191]	-1608	276.5	18	59
449	G[189]	-1629	354.5	18	59
450	G[187]	-1650	276.5	18	59
451	G[185]	-1671	354.5	18	59
452	G[183]	-1692	276.5	18	59
453	G[181]	-1713	354.5	18	59
454	G[179]	-1734	276.5	18	59
455	G[177]	-1755	354.5	18	59
456	G[175]	-1776	276.5	18	59
457	G[173]	-1797	354.5	18	59
458	G[171]	-1818	276.5	18	59
459	G[169]	-1839	354.5	18	59
460	G[167]	-1860	276.5	18	59
461	G[165]	-1881	354.5	18	59
462	G[163]	-1902	276.5	18	59
463	G[161]	-1923	354.5	18	59
464	G[159]	-1944	276.5	18	59
465	G[157]	-1965	354.5	18	59
466	G[155]	-1986	276.5	18	59
467	G[153]	-2007	354.5	18	59
468	G[151]	-2028	276.5	18	59
469	G[149]	-2049	354.5	18	59
470	G[147]	-2070	276.5	18	59
471	G[145]	-2091	354.5	18	59
472	G[143]	-2112	276.5	18	59
473	G[141]	-2133	354.5	18	59
474	G[139]	-2154	276.5	18	59
475	G[137]	-2175	354.5	18	59
476	G[135]	-2196	276.5	18	59

No.	Name	X-axis	Y-axis	W	H
477	G[133]	-2217	354.5	18	59
478	G[131]	-2238	276.5	18	59
479	G[129]	-2259	354.5	18	59
480	G[127]	-2280	276.5	18	59
481	G[125]	-2301	354.5	18	59
482	G[123]	-2322	276.5	18	59
483	G[121]	-2343	354.5	18	59
484	G[119]	-2364	276.5	18	59
485	G[117]	-2385	354.5	18	59
486	G[115]	-2406	276.5	18	59
487	G[113]	-2427	354.5	18	59
488	G[111]	-2448	276.5	18	59
489	G[109]	-2469	354.5	18	59
490	G[107]	-2490	276.5	18	59
491	G[105]	-2511	354.5	18	59
492	G[103]	-2532	276.5	18	59
493	G[101]	-2553	354.5	18	59
494	G[99]	-2574	276.5	18	59
495	G[97]	-2595	354.5	18	59
496	G[95]	-2616	276.5	18	59
497	G[93]	-2637	354.5	18	59
498	G[91]	-2658	276.5	18	59
499	G[89]	-2679	354.5	18	59
00	G[87]	-2700	276.5	18	59
501	G[85]	-2721	354.5	18	59
502	G[83]	-2742	276.5	18	59
503	G[81]	-2763	354.5	18	59
504	G[79]	-2784	276.5	18	59
505	G[77]	-2805	354.5	18	59
506	G[75]	-2826	276.5	18	59
507	G[73]	-2847	354.5	18	59
508	G[71]	-2868	276.5	18	59
509	G[69]	-2889	354.5	18	59
510	G[67]	-2910	276.5	18	59
511	G[65]	-2931	354.5	18	59
512	G[63]	-2952	276.5	18	59
513	G[61]	-2973	354.5	18	59
514	G[59]	-2994	276.5	18	59
515	G[57]	-3015	354.5	18	59
516	G[55]	-3036	276.5	18	59
517	G[53]	-3057	354.5	18	59
518	G[51]	-3078	276.5	18	59
519	G[49]	-3099	354.5	18	59
520	G[47]	-3120	276.5	18	59
521	G[45]	-3141	354.5	18	59
522	G[43]	-3162	276.5	18	59
523	G[41]	-3183	354.5	18	59
524	G[39]	-3204	276.5	18	59
525	G[37]	-3225	354.5	18	59
526	G[35]	-3246	276.5	18	59
527	G[33]	-3267	354.5	18	59
528	G[31]	-3288	276.5	18	59
529	G[29]	-3309	354.5	18	59
530	G[27]	-3330	276.5	18	59
531	G[25]	-3351	354.5	18	59
532	G[23]	-3372	276.5	18	59
533	G[21]	-3393	354.5	18	59
534	G[19]	-3414	276.5	18	59
535	G[17]	-3435	354.5	18	59
536	G[15]	-3456	276.5	18	59

No.	Name	X-axis	Y-axis	W	H
537	G[13]	-3477	354.5	18	59
538	G[11]	-3498	276.5	18	59
539	G[9]	-3519	354.5	18	59
540	G[7]	-3540	276.5	18	59
541	G[5]	-3561	354.5	18	59
542	G[3]	-3582	276.5	18	59
543	G[1]	-3603	354.5	18	59
544	T_N18V	-3624	276.5	18	59
545	T_N18V	-3645	354.5	18	59
546	AL_L	-3627	-327	110	110
547	AL_R	3627	-327	110	110

13. REVISION HISTORY

Revision	Content	Page	Date
1.0.1	JD79666 datasheet 1st version	-	2023/06/13
1.0.2	Updated Bump information		2023/06/14
1.0.3	Modify test pin name	-	2023/06/19
1.0.4	Modify project name: JD79676	-	2023/07/06