



## 4.26 inch E-paper Display Serie

**GDEQ0426T82-FL01C**

Dalian Good Display Co., Ltd.



# Product Specifications



<b>Customer</b>	<b>Standard</b>
<b>Description</b>	<b>4.26" EPD with Front-light</b>
<b>Model Name</b>	<b>GDEQ0426T82-FL01C</b>
<b>Date</b>	<b>2025/10/05</b>
<b>Revision</b>	<b>1.0</b>

	Design Team		
	Approval	Check	Edit
			

**NO.18 Zhonghua W. Rd, Ganjingzi Dist, Dalian, China**

**Tel: +86-411-84619565**

**Email: info@good-display.com**

**Site: www.good-display.com**

# Content

1. Overview.....	4
2. Features.....	4
3. Mechanical Specification.....	4
4. Mechanical Drawing of EPD Module.....	5
5. Input/output Pin Assignment.....	6
6. Absolute maximum rating.....	7
7. Electrical Characteristics.....	7
7.1 DC Characteristics.....	7
7.2 Panel DC Characteristics.....	8
7.3 Optical Specification.....	8
7.4 AC Electrical Characteristics.....	9
8. Functional Specification and Application Circuit.....	10
8.1 Power On/Off and DSLP Sequence.....	10
8.2 Reference Circuit.....	11
9. Matched Development Kit.....	12
10. Reliability Test.....	13
11. Outgoing Quality Control Specifications.....	14
12. Handling, Safety and Environmental Requirements.....	20
13. Packing.....	22
14. Precautions.....	23

## 1 Overview

The GDEQ0426T82-FL01C is a 4.26-inch reflective electrophoretic display module with a front-light, built on an active matrix TFT substrate. It features an 800x480 pixel resolution and can display 1-bit black-and-white images based on the associated lookup table. The panel integrates a gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memory for storing the frame buffer and lookup tables. Additional circuitry allows control of VCOM and border settings for enhanced performance.

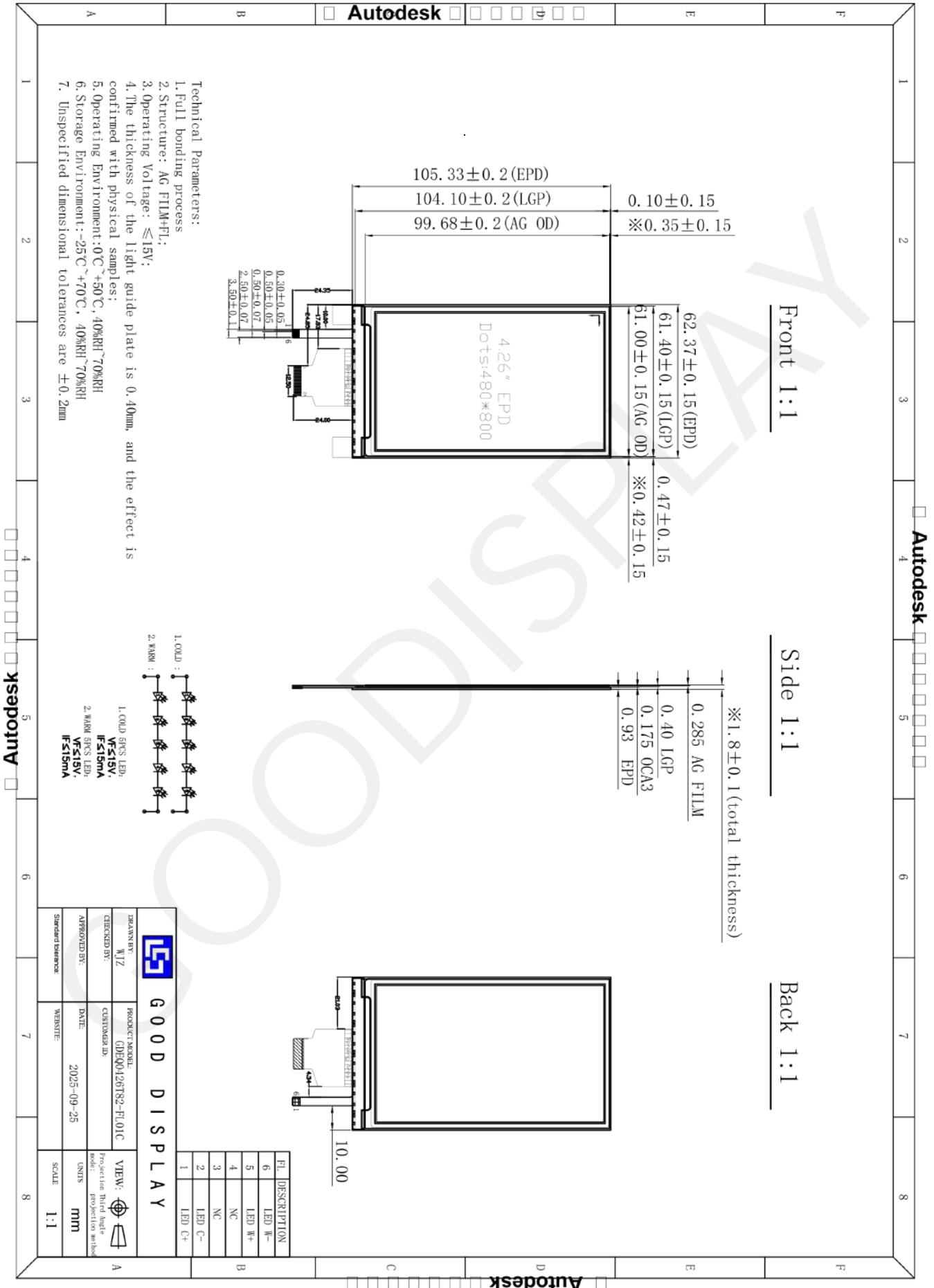
## 2 Features

- Ultra wide viewing angle
- Ultra low power consumption
- I<sup>2</sup>C Signal Master Interface to read external temperature sensor.
- On chip display RAM
- Interface :4-Wire SPI or 3-Wire SPI
- Wide range of operating temperature: 0°C to 50°C
- Wide range of storage temperature: -25°C to 70°C
- High reflectance and contrast TFT electrophoretic.
- With LED front-light. 5 dies in serial, 15V(Typ.)

## 3 Mechanical Specifications

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	800(H)×480(V)	-
2	Screen Size	4.26	Inch
3	Active Area	92.8(H)×55.68(V)	mm
4	Pixel Pitch	0.116×0.116	mm
5	Color	Black and White	
6	Outline Dimension	105.33(H) × 62.37(V) × 1.8(D)	mm
7	Pixel Configuration	Square	-
8	Driver IC	SSD1677	-
9	Module Weight	20.70±10%	gram

### 4 Mechanical Drawing of EPD module



## 5. Module Interface

PIN NO.	PIN NAME	DESCRIPTION
1,4	NC	No Connection
2	GDR	This pin is N-Channel MOSFET gate drive control pin.
3	RESE	Current Sense Input for the control loop
5	VSH2	This pin is Positive Source driving voltage, VSH2 Connect a stabilizing capacitor between VSH2 and VSS in the application circuit.
6	NC	No Connection
7	NC	No Connection
8	BS1	This pin is for selecting 3-wire(H active) or 4-wire(L active) SPI interface.
9	BUSY	This pin is Busy state output pin. When Busy is High, the operation of the chip should not be interrupted, and command should not be sent. For example, The chip would output Busy pin as High when <ul style="list-style-type: none"> <li>- Outputting display waveform; or</li> <li>- Programming with OTP</li> </ul> Communicating with digital temperature sensor In the cascade mode, the BUSY pin of the slave chip should be left open.
10	RES#	This pin is reset signal input (Active Low).
11	D/C#	This pin is Data/Command control pin connecting to the MCU
12	CS#	This pin is the chip select input connecting to the MCU.
13	SCL	This pin is serial clock pin for interface.
14	SDA	This pin is serial data pin for interface.
15	VDDIO	Power for interface logic pins
16	VCI	Power input pin for the chip.
17	VSS	Ground
18	VDD	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS under all circumstances
19	VPP	Power Supply for OTP Programming.
20	VSH1	This pin is Positive Source driving voltage, VSH1 Connect a stabilizing capacitor between VSH1 and VSS in the application circuit.
21	VGH	This pin is Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and VSS in the application circuit.
22	VSL	This pin is Negative Source driving voltage. Connect a stabilizing capacitor between VSL and VSS in the application circuit.
23	VGL	This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and VSS in the application circuit.
24	VCOM	This pins is VCOM driving voltage Connect a stabilizing capacitor between VCOM and VSS in the application circuit.

## 6 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	VCI	-0.5	+4.0	V	-
Logic Input voltage	VIN	-0.5	VDDIO+0.5	V	-
Logic Output voltage	VOUT	-0.5	VDDIO+0.5	V	-
Operating Temp.	Top	0	+50	C	-
Storage Temp	Tstg	-25	+70	C	-

Note (1): All of the voltages are on the basis of "VSS = 0V" .

Note (2): Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

## 7 Electrical Characteristics

### 7.1 DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.3V, TOPR =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCI operation voltage	VCI	-	-	2.2	3.3	3.6	V
High level input voltage	V <sub>IH</sub>	Digital input pins	-	0.8*VDDIO	-	VDDIO	V
Low level input voltage	V <sub>IL</sub>	Digital input pins	-	0	-	0.2*VDDIO	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = - 100uA	-	0.9*VDDIO	-	-	V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100uA	-	-	-	0.1*VDDIO	V
OTP Program voltage	VPP	-	-	7.25	7.5	7.75	V
Typical power panel	P <sub>TYP</sub>	VCI=3.3V	-	-	26.4	-	mW
Standby power panel	P <sub>STPY</sub>	VCI=3.3V	-	-	0.0066	-	mW
Typical operating current(white state)	Iopr_VCI	VCI=3.3V	-	-	8.0	-	mA
Full update time	-	23° C	-	-	3.5	-	sec
Fast update time	-	23° C	-	-	1.5	-	sec
Partial update time	-	23° C	-	-	0.42	-	sec
Sleep mode current	Islp_VCI	VCI=3.3V DC/DC OFF No clock No output load Ram data retain	VCI	-	40	70	uA
Deep sleep mode current	Idslp_VCI	VDD OFF	VCI	-	2	6	uA

Note: The VDD, VCI input must be kept in a stable value; ripple and noise are not allowed.

## 7.2 Panel DC Characteristics (Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.3V, TOPR =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-	-2.0	-	V
Positive Source output voltage	V <sub>SH</sub>	-	S <sub>0</sub> ~S <sub>479</sub>	-	15	-	V
Negative Source output voltage	V <sub>SL</sub>	-	S <sub>0</sub> ~S <sub>479</sub>	-	-15	-	V
Positive gate output voltage	V <sub>gh</sub>	-	G <sub>0</sub> ~G <sub>799</sub>	19.5	20	20.5	V
Negative gate output voltage	V <sub>gl</sub>	-	G <sub>0</sub> ~G <sub>799</sub>	-19.5	-20	-20.5	V

## 7.3 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	Note 1
CR	Contrast Ratio	indoor	8:1	-	-	-	Note 2
T update	Image update time	23 °C	-	4	-	sec	-
Tlife	Life	Topr	-	1000000 times or 5 years	-	-	-

Notes1: Luminance meter: Eye-One Pro Spectrophotometer.

Notes2:CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

### 7.4 AC Electrical Characteristics

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, TOPR = 25°C, CL=20Pf

**Write mode**

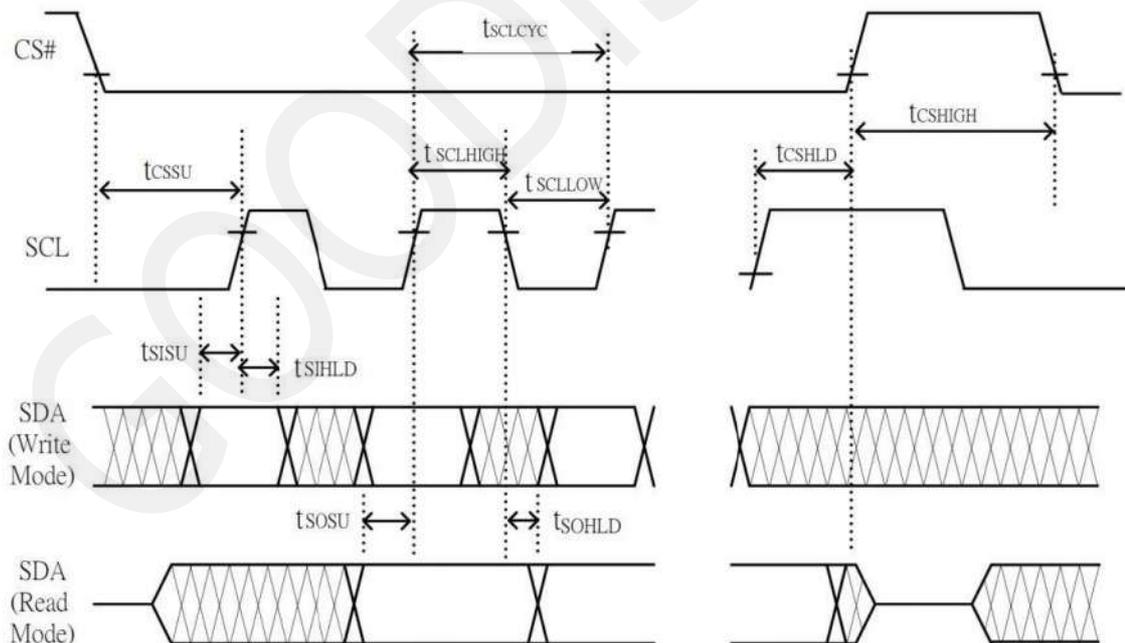
Symbol	Parameter	Min	Typ	Max	Unit
f <sub>SCL</sub>	SCL frequency (Write Mode)			20	MHz
t <sub>CSSU</sub>	Time CS# has to be low before the first rising edge of SCLK	20			ns
t <sub>CSHLD</sub>	Time CS# has to remain low after the last falling edge of SCLK	20			ns
t <sub>CSHIGH</sub>	Time CS# has to remain high between two transfers	100			ns
t <sub>SCLCYC</sub>	SCL cycle time	50			ns
t <sub>SCLHIGH</sub>	Part of the clock period where SCL has to remain high	25			ns
t <sub>SCLLOW</sub>	Part of the clock period where SCL has to remain low	25			ns
t <sub>SISU</sub>	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t <sub>SIHLD</sub>	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

**Read mode**

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>SCL</sub>	SCL frequency (Read Mode)			2.5	MHz
t <sub>CSSU</sub>	Time CS# has to be low before the first rising edge of SCLK	100			ns
t <sub>CSHLD</sub>	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t <sub>CSHIGH</sub>	Time CS# has to remain high between two transfers	250			ns
t <sub>SCLHIGH</sub>	Part of the clock period where SCL has to remain high	180			ns
t <sub>SCLLOW</sub>	Part of the clock period where SCL has to remain low	180			ns
t <sub>SOSU</sub>	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t <sub>SOHLD</sub>	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

SPI timing diagram

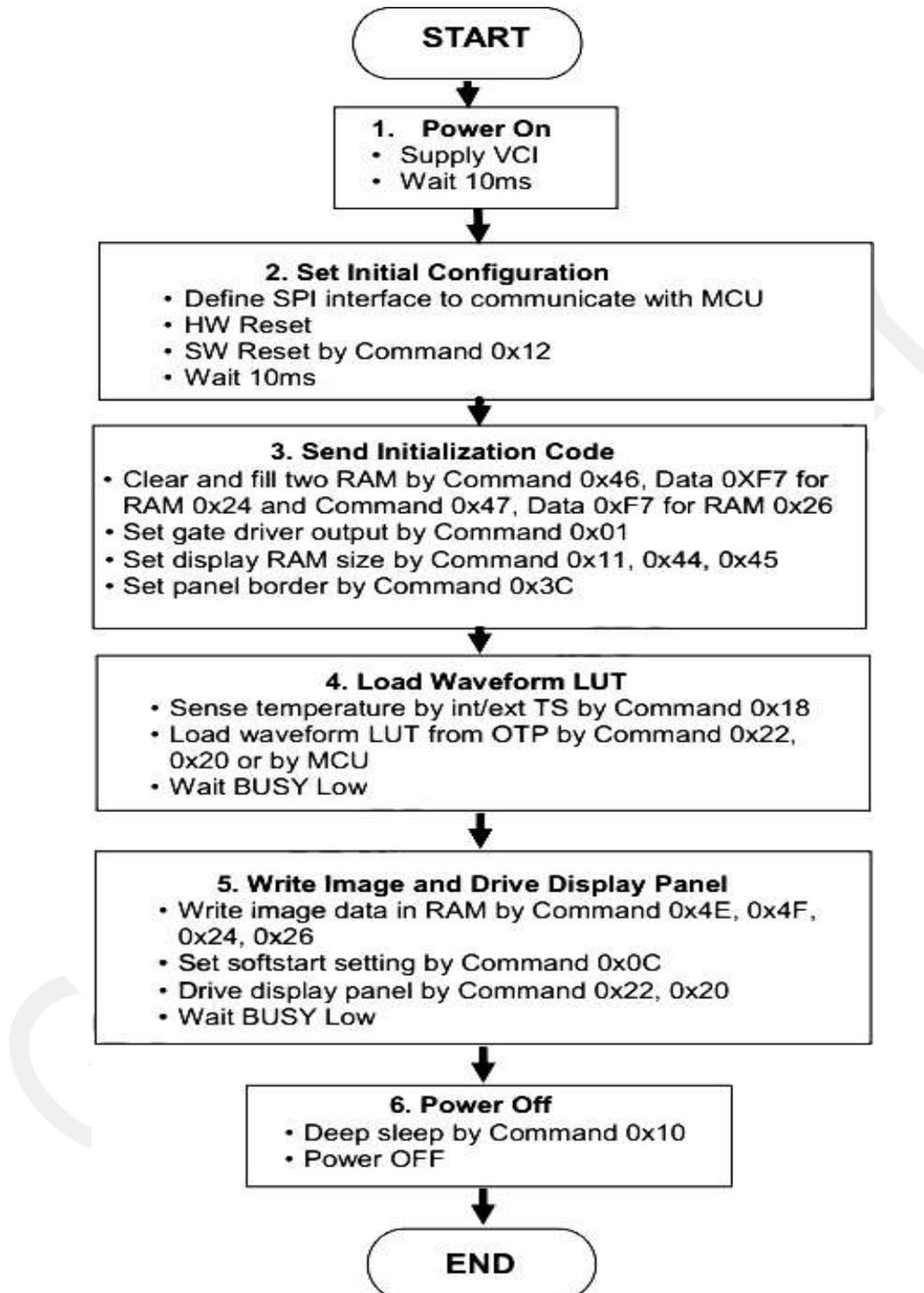


SPI interface timing

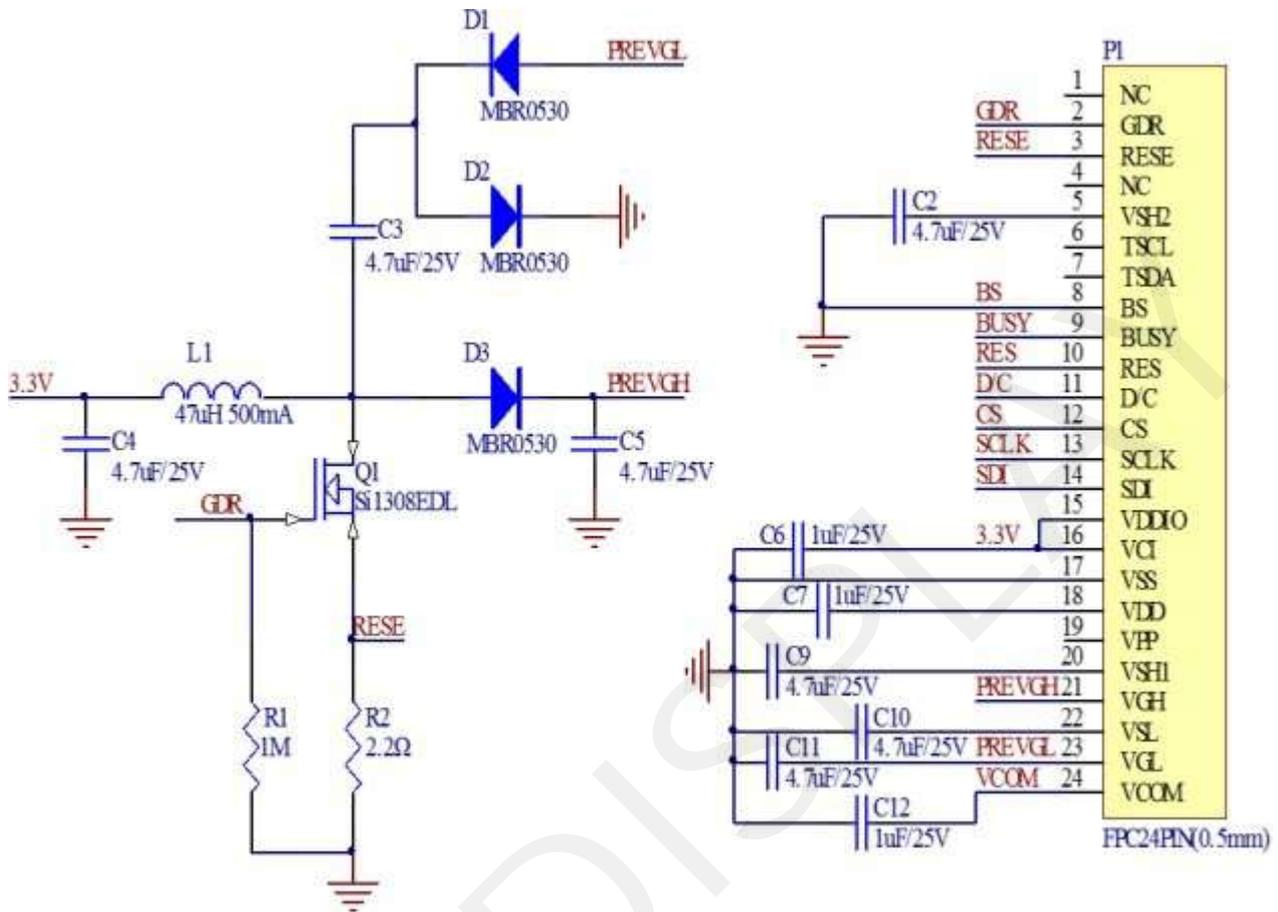
## 8 Functional Specification and Application Circuit

### 8.1 Power On/Off and DSLP Sequence

General operation flow to drive display panel



### 8.2 Reference Circuit



Part Name	Requirements for spare part
C1—C12	0603/0805; X5R/X7R; Voltage Rating: ≥25V
R1、R2	0603/0805; 1% variation, ≥0.05W
D1—D3	MBR0530: 1)Reverse DC Voltage ≥30V 2)Io ≥500mA 3)Forward voltage ≤430mV
Q1	Si1308EDL: 1)Drain-Source breakdown voltage ≥30V 2)Vgs(th) ≤1.5V 3)Rds(on) ≤400mΩ
L1	refer to NR3015: Io=500mA(max)
P1	24pins, 0.5mm pitch

## 9 Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) Good Display `s E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.

DESPI Development Kit consists of the development board and the pinboard . More details about the Development Kit, please click to the following link:

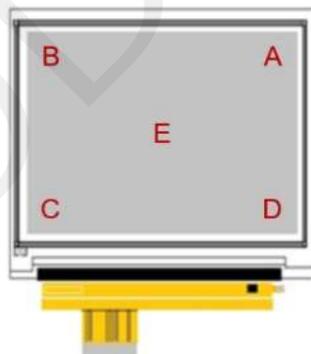
<https://www.good-display.com/product/219.html>

GOODDISPLAY

## 10 Reliability

NO	Test items	Test condition	QUANTITY
1	Low-Temperature Storage	T = -25°C , low temperature film T= -30°C; White screen state, for 240h.	5pcs
2	Low-Temperature Operation	T = 0°C, 240 h; Put the product into the experimental procedure, run it in the temperature box, and check it every 24 hours.	5pcs
3	High-Temperature Operation	T = 50°C, RH = 35%, 240 h; Put the product into the experimental procedure, run it in the temperature box, and check it every 24 hours.	5pcs
4	High-Temperature Storage	T=70°C , RH=40%; White screen state, for 240h.	5pcs
5	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min]; 100 cycles.	5pcs
6	High-Temperature/ High- humidity Storage	T=50°C , RH=90%; White screen state, for 240h.	5pcs
7	UV exposure Resistance	765W/m <sup>2</sup> for 168hrs,T = 40°C, RH=35%;	5pcs
8	ESD Contact discharge	±200V, Test 5 point; Each point discharge 10 times. Time interval is not less than 1 second.	5pcs

### ESD test location



### Test and measurement conditions

After the end of the experiment, the sample was taken out of the temperature chamber, and stood at room temperature for 1h, and then the sample was inspected for appearance, function and optical inspection.

### Criteria for qualification (pass the test if all qualified) :

- (1) The product can be normal refresh.
- (2) There are no new point defects or line defects in the display screen.
- (3) discoloration, blurred handwriting and barcode can be read on the complex screen.

## 11 Outgoing Quality Control Specifications

### 11.1 Sampling Method

- (1) GB/T 2828.1, inspection level II, normal inspection, single sample inspection
- (2) AQL: Major 0.4; Minor 0.65

### 11.2 Inspection Conditions

The environmental conditions for test and measurement are performed as follows. Temperature:  $23 \pm 3^\circ\text{C}$

Humidity:  $55 \pm 15\% \text{R.H}$

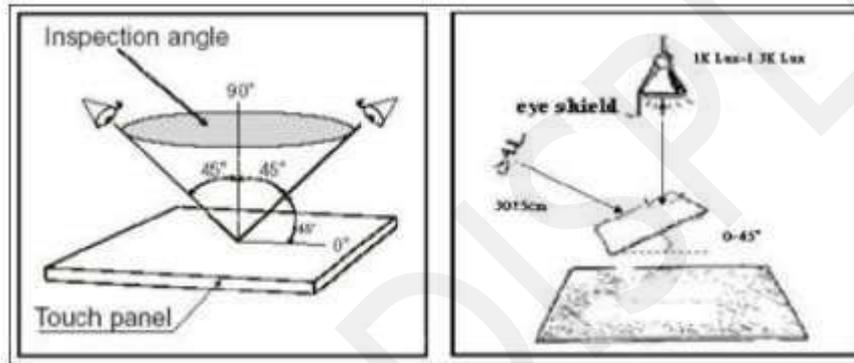
Inspection of illuminance: 800~1500Lux

Inspection time: signal face 5S-10S

Distance between the Panel & Eyes:  $30 \pm 10\text{cm}$

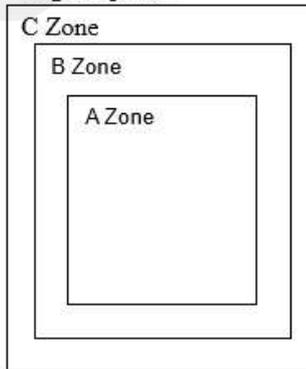
Viewing angle from the vertical in each direction:  $\pm 45^\circ$

(See the sketch below)



### 11.3 Quality Assurance Zones

Edge of panel



Zone A : Active Area

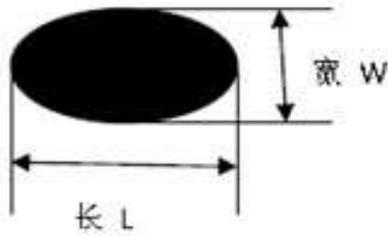
Zone B: Black Frame Area

Zone C: Outside Black Frame Area

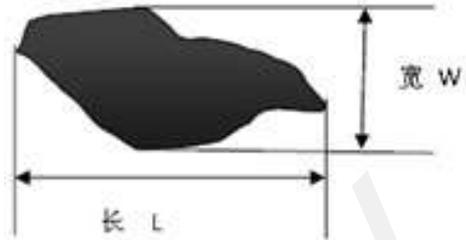
### 11.4 Inspection Standard

Defects Definition of  $\Phi$ &L&W (Unit: mm)

#### 11.4.1 Dot defects:

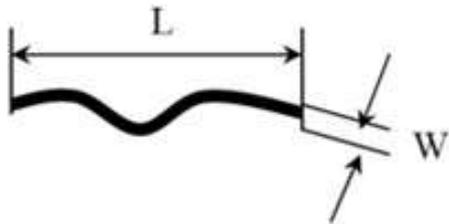


$$\Phi D = \text{Max}(L, W)$$

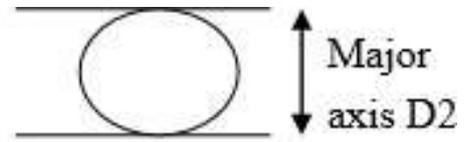
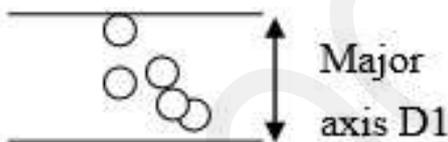


$$\Phi D = \text{Max}(L, W)$$

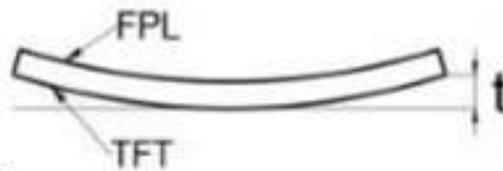
#### 11.4.2 line defect:



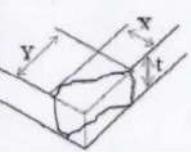
#### 11.4.3 Small bubble aggregation and large bubble definition:



#### 11.4.4 TFT warpage:



## 11.5 Appearance Defects

NO.	ITEM	CRITERIA	Acceptable range	Method	Defect level	Area
1	Spotty (black spots, white spots, foreign bodies, air bubbles, bumps)	$D \leq 0.25\text{mm}$	Ignore	Film Card	Minor	Zone A
		$0.25\text{mm} < D \leq 0.5 \text{ mm}$ , Distance $\geq 5\text{mm}$	$N \leq 4$			
		$D > 0.5 \text{ mm}$	$N = 0$			
		$0.1\text{mm} < D \leq 0.25 \text{ mm}$ (Dense point)	$N \leq 3/\text{cm}^2$			
2	POOR LINEAR SHAPE (foreign body, glass scratch)	$L \leq 2\text{mm}$ , $W \leq 0.1\text{mm}$	Ignore	Film Card	Minor	Zone A
		$2\text{mm} < L \leq 8\text{mm}$ , $0.1 < W \leq 0.5\text{mm}$	$N \leq 4$			
		$L > 8\text{mm}$ , $W > 0.5\text{mm}$ Note: FPL Lacerations are not allowed	$N = 0$			
	steel pit	Long strip pits are not allowed	$N = 0$	Sight Check	Minor	Zone A
3	Glass Crack	Extensional cracks are not allowed 	$N = 0$	Sight Check	Major	Zone B,C
4	Edge breakage	$X \leq 3\text{mm}$ , $Y \leq 0.5\text{mm}$ , It does not affect the electrode 	$N \leq 2$	Sight Check/ <u>Microsc</u> <u>ope</u>	Minor	Zone C
5	Chip Package Chip Off	$X \leq 2\text{mm} \cdot Y \leq 2\text{mm}$ , It does not affect the electrode(FPC edge) $X \leq 1\text{mm} \cdot Y \leq 1\text{mm}$ , It does not affect the electrode((Not FPC edge) 	$N \leq 2$	Sight Check/ <u>Microsc</u> <u>ope</u>	Minor	Zone C
6	Dirt	No dirt (finger print, dust, residual glue, etc.)	Ignore	Sight Check	Minor	Zone A,B
7	Silicone	The maximum diameter of a single bubble cannot exceed 2mm	$N \leq 2$	Sight Check/ Film card	Minor	Zone C
		Crack is not allowed and there are no visible impurities in the glue of the lead part	$N = 0$			
		The adhesive must completely cover the ACF, lead area and IC and should be applied evenly	$N = 0$			

NO.	ITEM	CRITERIA	Acceptable range	Method	Defect level	Area
		No glue leakage, no obvious lack of glue in the lead area	N=0			
		Glue height exceeds PS surface	N=0			
		FPC Front overflow glue width>0.5mm or Back side overflow glue width>1mm	N=0			
8	Edge Sealing Adhesive	No glue leakage	N=0	Sight Check/ Film card	Major	Zone C
		The height of sealant exceeds PS surface	N=0		Minor	
		The edge sealing adhesive shall not leak the TFT glass substrate	N=0			
		Judging Ok of water-blocking area $\geq 0.7$ mm of PS edge sealant	N=0		Minor	
9	Protective film	Foreign body in protective film	N=0	Sight Check	Minor	Zone A
		The protective film punctures and injures FPL	N=0			
10	Pull Tape	Attachment position is wrong Cannot tear up the protective film	N=0	Sight Check	Minor	Zone C
11	FPC	FPC has break, scratch, gold finger stripping or oxidation, dirty, residual glue	N=0	Sight Check	Major	Zone C
12	Glass edge bulge	$X \leq 3\text{mm} \cdot Y \leq 0.3\text{mm}$	$N \leq 1$	Sight Check	Minor	Zone C
13	Warping	$t > 1\text{mm}$ ( 3.5inch below ) $t > 3\text{mm}$ ( 3.5inch above )	N=0	Plug Gage	Minor	Zone C
14	Chromatism	Color difference in silver paste area (Not in Zone A)	Ignore	Sight Check	Minor	Zone C
		FPL Peeling occurs, chromatic aberration occurs	N=0	Sight Check	Major	Zone A,B
		The color difference of side loss of FPL in zone B $\geq 1/2$ width	N=0	Sight Check	Major	Zone A,B
15	Silver pulp point	FPL and TFT substrate conduction, silver point $< 1.0\text{mm}$ (Both single silver point and double silver point should meet this specification)	N=0	Film card	Major	Zone C
16	Inkjet code	The ink jet printing font is clear, identifiable, and cannot be missing	N=0	Sight Check	Minor	Zone C

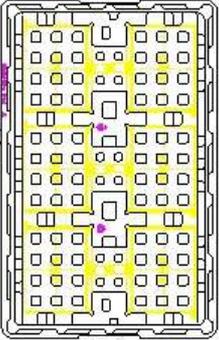
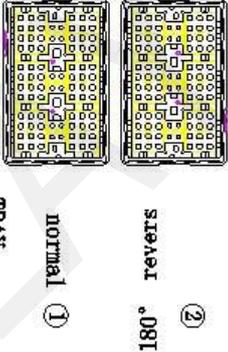
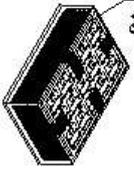
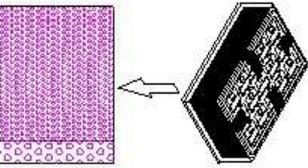
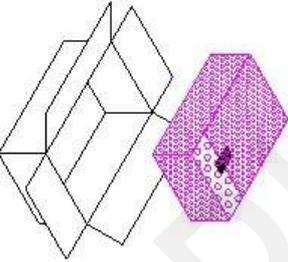
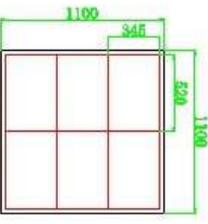
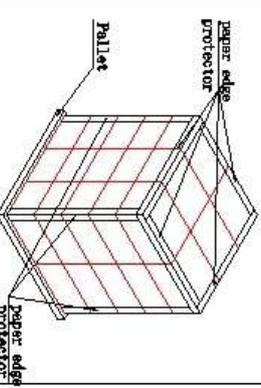
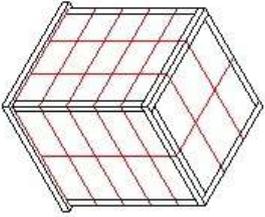
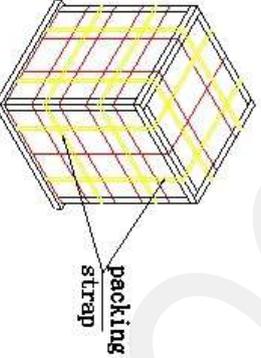
## 11.6 Displaying Defects

NO.	ITEM	CRITERIA	Acceptable range	Method	Defect level	Area
1	Poor DOT SHAPE (black, white, group White)	$D \leq 0.25\text{mm}$	Ignore	Film Card	Major	Zone A
		$0.25\text{mm} < D \leq 0.5\text{mm}$ , Distance $\geq 5\text{mm}$	$N \leq 4$			
		$D > 0.5\text{mm}$	$N = 0$			
		$0.1\text{mm} < D \leq 0.25\text{mm}$ (Dense point)	$N \leq 3/\text{cm}^2$			
2	Line defects 	White or black lines running through the entire screen under any operation interface	$N = 0$	Sight Check	Major	Zone A
3	<u>ghost</u>	Ghosts appear only during screen switching	Ignore	Sight Check	Major	Zone A
4	Flash Point	Flash point occurs during screen switching only	Ignore	Sight Check	Major	Zone A
5	Flash Line	Flash line occurs during screen switching only	$N = 0$	Sight Check	Major	Zone A
6	Display screen error	Unable to display a fixed screen correctly	$N = 0$	Sight Check	Major	Zone A
7	Display abnormal	No display, The red matrix darkens, Note fuzzy, bar code can not be scanned,	$N = 0$	Sight Check	Major	Zone A
8	Residual image	Residual Image Inspection (visual, final judgment reference optical specification)	$N = 0$	Sight Check	Major	Zone A
9	Mura Anomaly	White/gray. Mura doesn't allow it	$N = 0$	Sight Check	Major	Zone A

### 11.7 Identification and packaging inspection

NO.	ITEM	CRITERIA	Method	Defect level
1	Package	<ul style="list-style-type: none"> <li>(1). The products are completely placed in the anti-static tray without overlapping.</li> <li>(2). Products with different models cannot be mixed in one internal packaging bag.</li> <li>(3) There is a desiccant in the packaging bag, with good internal packaging and no expansion of the packaging bag.</li> <li>(4) The Tray model, quantity and way used for packaging meet the requirements of product specifications.</li> </ul>	Sight Check	Minor
2	Inner and outer packing	<ul style="list-style-type: none"> <li>(1) No obvious deformation, damage, dampness or dirt on the packing case;</li> <li>(2) The type, quantity and method of the packing case used shall meet the requirements of the product specification.</li> <li>(3) There is no font or unclear design in the outer packing box.</li> </ul>	Sight Check	Minor
3	Labels for inner and outer cases	<ul style="list-style-type: none"> <li>(1). Any unnecessary marks or marks are not allowed to exist;</li> <li>(2). The label information such as model, specification, quantity, weight, material number, month label and environmental protection label should be clear and correct, which should be in line with product specifications or marked according to customer requirements.</li> </ul>	Sight Check	Minor

## 12 Packing

Controlled Seal		Packing Process (1)~(12)					
(1)	 Detail A	(2)	 TRAY normal ① saver .081 ②	(3)	order ①、②、①、② fix trays with tape 186 pcs of 1 carton 1 tray contain 6 pcs 31 contained trays, 1 empty tray 	(4)	package with plastic bags add five desiccants create a power vacuum *5 
(5)	After tray be packed, wrap the package in a bubble bag and seal with scotch tape. 	(6)		(7)	31 contained trays, 1 empty Package quantity products: 186 pcs of 1 carton.  ROHS Package finished	(8)	Pallet stack Pallet Type: 1100*1100*150mm Plastic Pallet 
(9)	Use paper edge protector Top face paper edge protector type : P213010-KC-A Side 1000*900*6mm, 7*16mm Side face paper edge protector type : P213010-WZ-A Side 1000*900*6mm, 7*16mm  paper edge protector Pallet paper edge protector	(10)	Finwind stretch film Wrap 3 layers of stretch film around the paper sheets (All around and on top), Wrap paper pallets, pallets, and boxes underneath 	(11)	Pack packing strap The packing tape should be tied to the cartons. If Stack height greater than or equal to 3 layers, 2 turns in length, width and height; If the stack height is less than 3 layers, the height direction is not used pack.  packing strap	(12)	Pack packing strap The surface of the packing belt shall not be twisted, skewed or cracked. After the packaging is completed, the tightness of the packaging belt is suitable. Use the packing iron buckle to fix the belt and cut off the excess packaging belt. The remaining amount is less than or equal to 20mm 

NOTE:1、The inner cartoster carton must be sealed with adhesive tape.

- 2、Fill up the gap with empty tray.
- 3、If the customer has special needs with the RoHS making, the inner carton and master carton need adhesive new RoHS marking at ●.
- 4、Packaging materials are not recommended for recycling.

## 13 Environmental

### 13.1 Handling, Safety and Environmental Requirements

<b>WARNING</b>
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

<b>CAUTION</b>
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged.

Moreover the display is sensitive to static electricity and other rough environmental conditions.

<b>Mounting Precautions</b>	
(1)	It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2)	It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3)	You should adopt radiation structure to satisfy the temperature specification.
(4)	Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5)	Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6)	When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7)	Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.
Product specification	The data sheet contains final product specifications.

**Limiting values**

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information**

Where application information is given, it is advisory and does not form part of the specification.

**Product Environmental certification**

ROHS

**REMARK**

All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

## 14 Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.
- (6) For more precautions, please click on the link:  
<https://www.good-display.com/news/80.html>