3.5 inch
E-paper Display Series

GDEM035T81

Dalian Good Display Co., Ltd.

GooDisplay®

Product Specifications

Customer	**Standard**
Description	**3.5" E-PAPER DISPLAY**
Model Name	**GDEM035T81**
Date	**2025/03/ 12**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
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1. over view

GDEM035T81 is an Active Matrix Electrophoretic Display(AMEPD), with interface and a reference system design. The display is capable to display images at 1-bit white and black full display capabilities. The 3.52inch active area contains 384x 184 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic shelfLabel (ESL) system.

2. Features

◆384x 184 pixels display
◆High contrast High reflectance
◆ultra wide viewing angle ultra low power consumption
◆pure reflective mode
◆Bi-stable display
◆commercial temperature range
◆Landscape portrait modes
◆Hard-coat antiglare display surface
◆ultra Low current deep sleep mode
◆on chip display RAM
◆waveform can stored in on-chip OTP Or written by MCU
◆serial peripheral interface available
◆on-chip oscillator
◆on-chip booster and regulator control for generating vcoM, Gate and source driving voltage
◆I2C Signal master interface to read external temperaturesensor
◆Built-in temperature sensor

3. Mechanical and optical specification

parameter	Specifications	unit	Remark
screen size	3.5	Inch	
Display Resolution	384(V) × 184(H)	pixel	DPI: 120
Active Area	38.18x79.68	mm	
pixel pitch	0 207x0 207	mm	
pixel configuration	Rectangle		
outline Dimension	45.03(H)×91.75 (V) xO.90(D)	mm	
weight	7.0±0.3	g	

symbol	parameter	conditions	Min	TYP.	Max	units	Notes
KS	Black state L* value		-	18	20		3-1
	Black Ghosting ΔL		-	1	-		3-1
WS	white state L* value		66	67	-		3-1
	white Ghosting ΔL		-	1	-		3-1
R	white Reflectivity	white	30	34	-	%	3-1
CR	contrast Ratio	Indoor	15:1	20:1	-		3-1 3-2
GN	2Grey Level	-	-	-	-		
Life		Temp:23±3ec Humidity:55±10%RH		5years			3-3

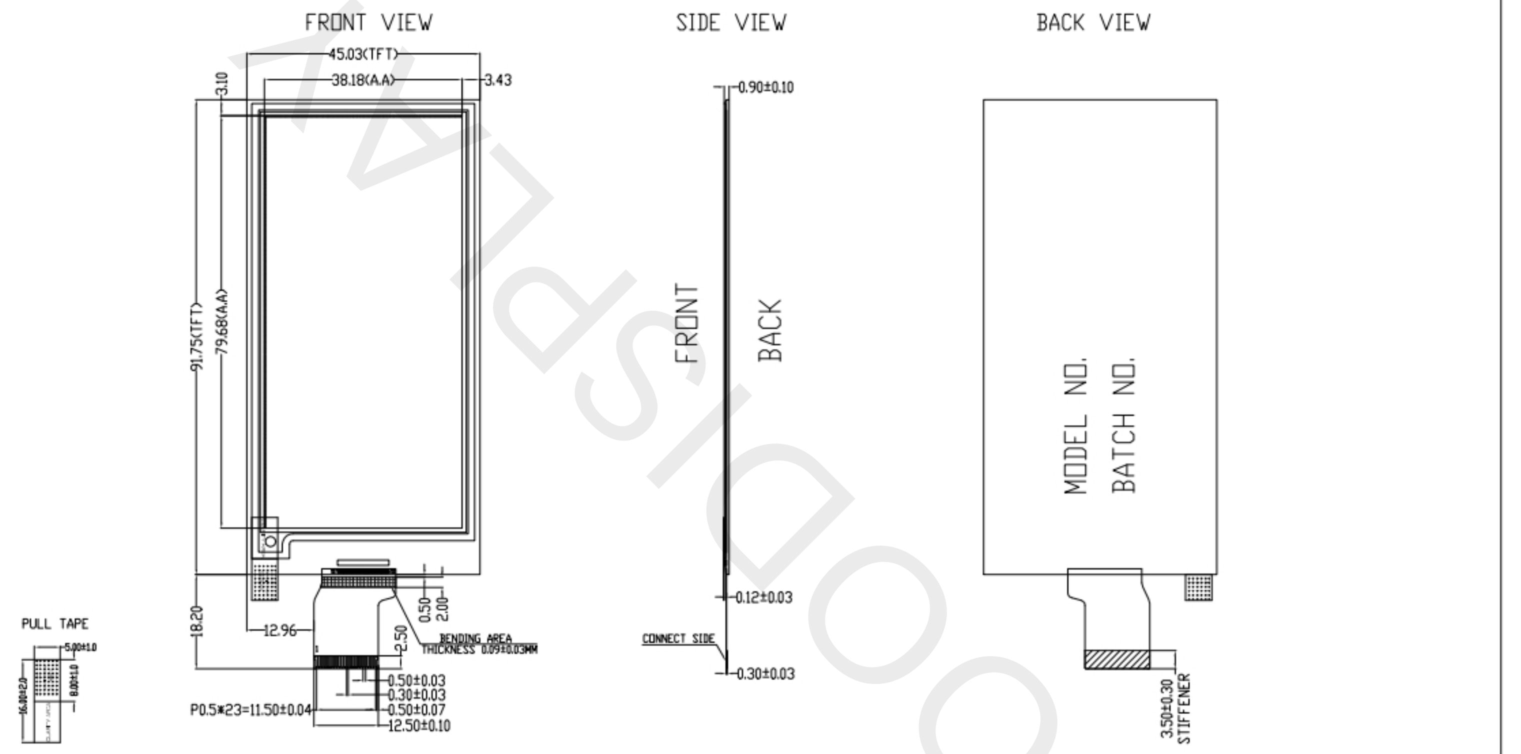
Notes: 3-1. Luminance meter: Eye-one pro spectrophotometer.

3-2. CR=surface Reflectance with all white pixel/surface Reflectance with all black pixels.

3-3. when the product is stored. The display screen should be kept white and face up.

4.Mechanical Drawing of EPD Module

Confirmation:



NOTE
1 DISPLAY MODULE 3.5″ ARRAY FOR EPD
2 DRIVER IC:SSD1685
3 RESOLUTION:184sourceX384gate
4 PIXEL SIZE:0.2075mmX0.2075mm

DATE:	TITLE:	PROJECT:	UNIT :	REV,:	3RD ANGLE :	TOLERANCES UNMARKED
25.03.13	EPD	GDEM035T81	mm	A	⌖	ANGLES±5° .X=±0.4mm .XX=±0.20mm .XXX=±0.20mm

5.Input/output pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other Nc pins	keep open
2	GDR	O	N-channel MOSFET Gate Drive control	
3	RESE	I	current sense Input for the control LooP	
4	NC	NC	Do not connect with other Nc pins	keep open
5	VSH2	C	positive source driving voltage 2	
6	TSCL	O	I2c Interface to digital temperature sensor clockpin	Note 5-6
7	TSDA	I/O	I2c Interface to digital temperature sensor Data pin	Note 5-6
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	BusY State outputpin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /command control pin	Note 5-2
12	CS#	I	chip select input pin	Note 5-I
13	SCL	I	serial clock pin (SPI)	
14	SDA	I/O	serial Data pin (SPI)	
15	VDDIO	P	power supply for interface logic pins It should be connected with vcl	
16	VCI	P	power supply for the chip	
17	VSS	P	Ground	
18	VDD	C	core logic power pin VDD Can be regulated internally from VCI. A Capacitor should be connected between VDD and vss	
19	VPP	P	FOR TEST	keep open
20	VSH1	C	positive source driving voltage	
21	VGH	C	power supplypin for positive Gate driving voltage and VSH1	
22	VSL	C	Negative source driving voltage	
23	VGL	C	power supplypin for Negative Gate driving voltage VCOM and vsL	
24	VCOM	C	VCOM driving voltage	

I = Input pin, O =output pin, I/o = Bi-directional pin (Input/output), P = power pin, C = capacitor pin

Note 5-1: This pin (cs#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when Cs#is pulled LOW.

Note 5-2: This pin is (D/C#) Data/command control pin connecting to the Mcu in 4-wire SPI mode. when the pin is pulled HIGH, the data at SDA Will be interpreted as data. when the pin is pulled LOW, the data at SDA Will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is BusY State output pin. when Busy is High, the operation ofchip should not be interrupted, command should not be sent. The chip would put Busy pin High when -outputting display waveform -communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

Note 5-6:This pin connect to the vss ifthere is no external temperature sensor.

BS1 state	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical characteristics

6.1Absolute Maximum Rating

parameter	symbol	Rating	unit
Logic supply voltage	VCI	-0.5 to +6.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic output voltage	VOUT	-0.5 to VCI +0.5	V
operating Temp range	TOPR	0 to +50	oc.
storage Temp range	TSTG	-25 to+70	oc.
optimal storage Temp	TSTGo	23±3	oc.
optimal storage Humidity	HSTGo	55±10	RH

Note:

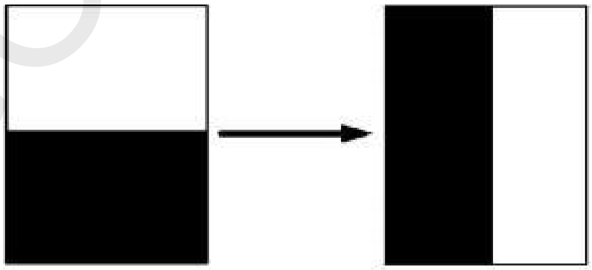
1. Maximum ratings are those values beyond which damages to the device may occur.Functional operation should be restricted to the limits in the panel Dc characteristics tables.

6.2 panel Dc characteristics

The following specifications apply for: Vss=0v, VCI=3.ov, TOPR = 25oc.

parameter	symbol	condition	Applicable pin	Min.	TYP.	Max.	unit
single ground	VSS	-		-	0	-	V
Logic supply voltage	VCI	-	VCI	2.2	3.0	3.7	V
core logic voltage	VDD		VDD	1.7	1.8	1.9	V
High level input voltage	VIH	-	-	0.8 VCI	-	-	V
Low level input voltage	VIL	-	-	-	-	0.2 VCI	V
High level output voltage	VOH	IOH = -100UA	-	0.9 VCI	-	-	V
Low level output voltage	Voc	IOL = 100UA	-	-	-	0.1 VCI	V
Typical power	PTYP	vcr =3.oV	-	-	15	-	mw
Deep sleep mode	PSTPY	vcr =3.oV	-	-	0.003	-	mw
Typical operating current	lopr_VCI	vcr =3.oV	-	-	5	- -	mA
Image update time	-	25 oc	-	-	4	-	sec
Typical peak current	lopr_VCI	2.2~3.7V			40	50	mA
Minimum power consumption spec	-	OC	-	-	-	80	mAs
	-	10C	-	-	-	60	mAs
	-	25oc	-	-	-	42	mAs
sleep mode current	Islp_VCI	DC/DC Off No clock No input load Ram data retain	-	-	20		UA
Deep sleep mode current	Idslp_vci	DC/DC Off No clock No input load Ram data not retain	-	-	1	5	UA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical characteristics are only guaranteed under the controller & waveform provided by DKE.

4. Electrical measurement: Tektronix oscilloscope - MD03024,

Tektronix current probe - TCP0030A·

6.3 panel Dc characteristics(DriverIC Internal Regulators)

The following specifications apply for: Vss=0v, VCI=3.ov, TOPR =25oc.

parameter	symbol	condition	Applicable pin	Min.	TYP.	Max.	unit
VcOM Output voltage	VCOM	-	VCOM	-	TBD	-	V
positive source output voltage	VSH	-	S0~S199	+14.5	+15	+15.5	V
Negative source output voltage	VSL	-	SO~S199	-15.5	-15	-14.5	V
positive gate output voltage	vgh	-	Go~G299	+19	+20	+21	V
Negative gate output voltage	vgl	-	Go~G299	-21	-20	-19	V

Notes: VGH, VGL, VSH, VSL drop voltage<2V.

6.4 panel AC Characteristics

6.4.1 MCU Interface selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI Or 3-wire SPI interface mode.

pin Name	Data/command Interface		control signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

6.4.2 Mcu serial Interface (4-wire SPI)

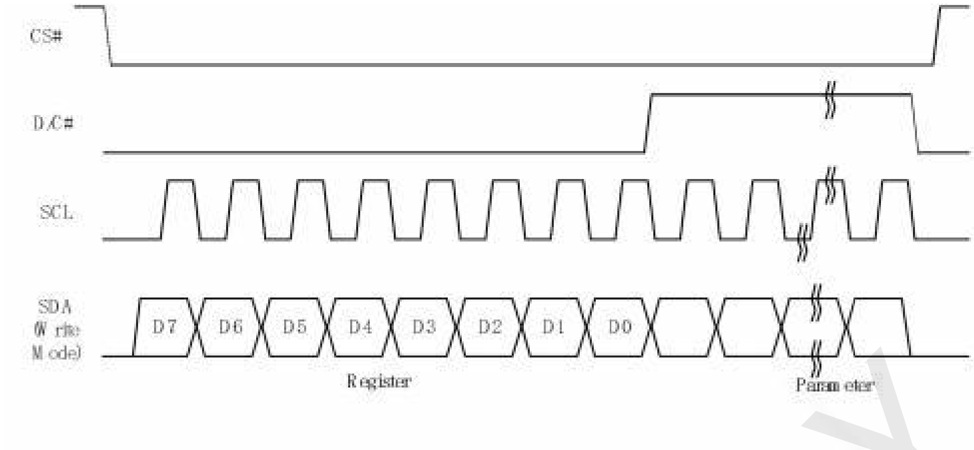
The serial interface consists of serial clock SCL, serial data SDA, D/c#, Cs#· This interface supports write mode and Read mode.

Function	CS#	D/C#	SCL
write command	L	L	↑
write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of scL in the order of D7, D6,... DO. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C#pin.

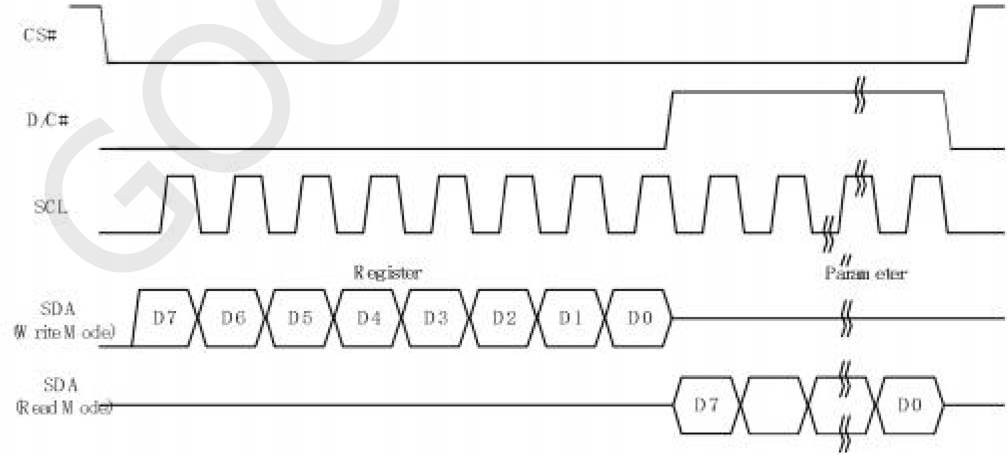
Figure 6-1: write procedure in 4-wire SPI mode



In the Read mode:

1. After driving cs# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6,… DO With D/C#keep low.
3. After SCL Change to low for the last bit ofregister, D/c# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of scL in the order ofD7, D6, …. DO.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, Cs# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode



6.4.3 Mcu serial Interface (3-wire SPI)

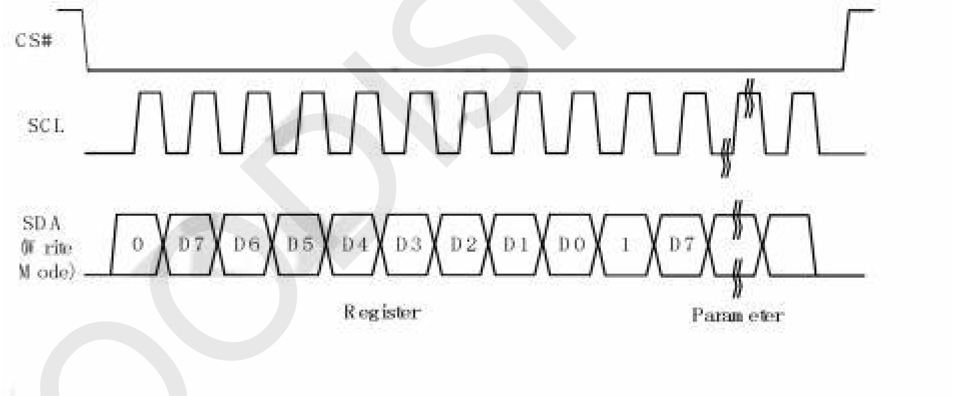
The 3-wire serial interface consists ofserial clock scL, serial data SDA and cs#. This interface also supports write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/c#bit, D7 to DO bit. The D/C# bit (first bit ofthe sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/c#bit = 1) or the command register (D/c#bit = 0).

Function	CS#	D/C#	SCL
write command	L	Tie	↑
write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

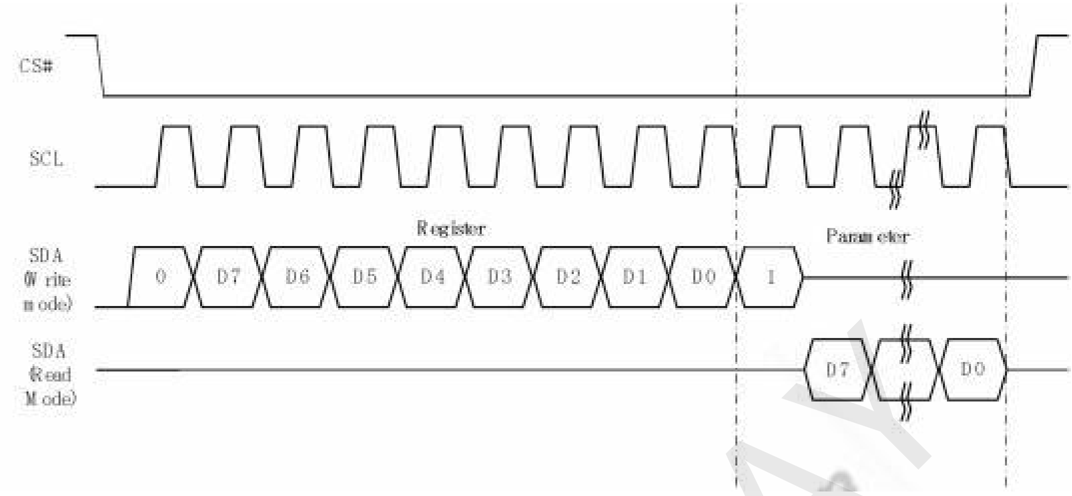
Figure 6-3: write procedure in 3-wire SPI mode



In the Read mode:

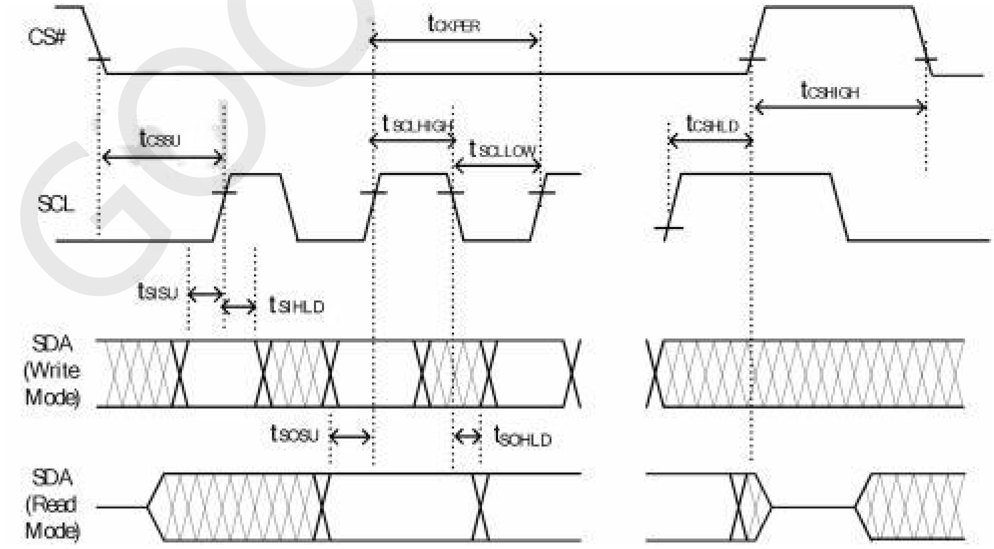
1. After driving cs# to low, MCU need to define the register to be read.
2. D/c=0 is shifted thru SDA With one rising edge of scL
3. SDA is shifted into an 8-bit shift register on every rising edge of scL in the order of D7, D6, ... DO.
4. D/c=1 is shifted thru SDA With one rising edge of scL
5. SDA is shifted out an 8-bit data on every falling edge ofscL in the order ofD7, D6, ... DO.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, Cs# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode



6.4.4 Interface Timing

The following specifications apply for: Vss=0v, VCI=3 .ov, TOPR =25oc.



changed Diagram

serial Interface Timing characteristics

(VCI - VSS = 2.2v to 3.7V, TOPR = 25OC, CL=20PF)

write mode

symbol	parameter	Min	TYP	Max	unit
fscL	SCL frequency (write Mode)			20	MHz
tcssu	Time Cs#has to be low before the first rising edge of scLK	60			ns
tcsHLD	Time Cs#has to remain low after the last falling edge of scLK	65			ns
tcsHIGH	Time Cs#has to remain high between two transfers	100			ns
tscLHIGH	part ofthe clock period where SCL has to remain high	25			ns
tscLLOW	part ofthe clock period where SCL has to remain low	25			ns
tsISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tsIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

symbol	parameter	Min	TYP.	Max	unit
fscL	SCL frequency (Read Mode)			2.5	MHz
tcssu	Time Cs#has to be low before the first rising edge of scLK	100			ns
tcsHLD	Time Cs#has to remain low after the last falling edge ofscLK	50			ns
tcsHIGH	Time Cs#has to remain high betwweentwwo transfers	250			ns
tscLHIGH	part ofthe clock period where SCL has to remain high	180			ns
tscLLOW	part ofthe clock period where SCL has to remain low	180			ns
tsosu	Time So(SDA Read Mode) wil1 be stable before the next rising edge ofscL		50		ns
tsoHLD	Time So (SDA Read Mode) will remain stable after the falling edge ofscL		0		ns

7.command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	DO	command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver output control	Gate setting A[8:0] = 012Bh [POR], 300 MUX MUX Gate lines setting as (A[8:0] + 1). B [2:0] = 0000 [POR]. Gate scanning sequence and direction B[2]: GD selects the 1st output Gate GD=0 [POR], GO is the 1st gate output channel, gate output sequence is G0, G1 , G2, G3, … GD= 1, G1 is the lst gate output channel, gate output sequence is G1 , G0, G3, G2, … B[1]: SM change scanning order ofgate driver. SM=0 [POR], G0, G1 , G2, G3 __G382, G299 (1eft and right gate interlaced) SM=l, G0, G2, G4 __G382, G1 , G3, __G299 B[0]: TB TB = 0 [POR], scan from GO to G299 TB = 1 , scan from G299 to GO.
0	1		A7	A6	A5	A4	A3	A2	A1	AO		
0	1		0	0	0	0	0	0	0	A8		
0	1		0	0	0	0	0	B2	B1	BO		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage control	set Gate Driving voltage A[4:0] = 17h[POR],VGH at20V[POR] VGH Setting from 10v to 20v
0	1		0	0	0	A4	A3	A2	A1	AO		
0	0	04	0	0	0	0	0	1	0	0	source Driving voltage control	set source Driving voltage A[7:0] = 41h[POR],VSH1 at 15V B[7:0] =Ach[POR],VSH2 at 5.4V C[7:0] = 32h[POR], VSL at - 15V
0	1		A7	A6	A5	A4	A3	A2	A1	AO		
0	1		B7	B6	B5	B4	B3	B2	B1	BO		
0	1		C7	C6	C5	C4	C3	C2	C1	Co		

0	0	oc	0	0	0	0	1	1	0	0	Booster soft start control	Booster Enable with phase 1 , phase 2 and phase 3 for soft start current and duration setting. A[7:0] -> soft start setting for phase1 = 8Bh [POR] B[7:0] -> soft start setting for phase2 = 9ch [POR] C[7:0] -> soft start setting for phase3 = 96h [POR] D[7:0] -> Duration setting = OFh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:
0	1		1	A6	A5	A4	A3	A2	A1	Ao		
0	1		1	B6	B5	B4	B3	B2	B1	Bo		
0	1		1	C6	C5	C4	C3	C2	C1	Co		
0	1		0	0	D5	D4	D3	D2	D1	Do		

Bit[6:4]	Driving strength selection
000	1(weakest)
001	2
010	3
011	4
100	5
101	6
110	7
111	8(strongest)

Bit[3:0]	Min off Time setting of GDR [Time unit]
0000 ~ 0011	NA
0100	2.6
0101	3.2
0110	3.9
0111	4.6
1000	5.4
1001	6.3
1010	7.3
1011	8.4
1100	9.8
1101	11.5
1110	13.8
1111	16.5

D[5:0]: duration setting ofphase
D[5:4]: duration setting ofphase 3
D[3:2]: duration setting ofphase 2
D[1:0]: duration setting ofphase 1

Bit[1 :0]	Duration ofphase [Approximation]
00	10ms
01	20ms
10	30ms
11	40ms

0	0	10	0	0	0	1	0	0	0	0	Deep sleep mode	Deep sleep mode control A[1 :0] : Description 00 Normal Mode [POR] 01 Enter Deep sleep Mode 1 11 Enter Deep sleep Mode 2 After this command initiated, the chip wwill enter Deep sleep Mode, Busypad will keep output high. Remark: To Exit Deep sleep mode, user required to send HWRESET to the driver
0	1		0	0	0	0	0	0	A1	A0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1 :0] = ID[1 :0] Address automatic increment / decrement setting The setting ofincrementing or decrementing ofthe address counter can be made independently in each upper and lower bit ofthe address. 00 -y decrement, X decrement, 01 -y decrement, X increment, 10 -y increment, X decrement, 11 -y increment, X increment [POR] A[2] = AM set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1 , the address counter is updated in the y direction.
0	1		0	0	0	0	0	A2	A1	Ao		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep sleep Mode Note: RAM are unaffected by this command.
0	0	18	0	0	0	1	1	0	0	0	Temperature sensor control	Temperature sensor selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor
			A7	A6	A5	A4	A3	A2	A1	AO		
0	0	1A	0	0	0	1	1	0	1	0	Temperature sensor control (write to temperature register)	write to temperature register. A[7:0] = 7Fh [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	AO		

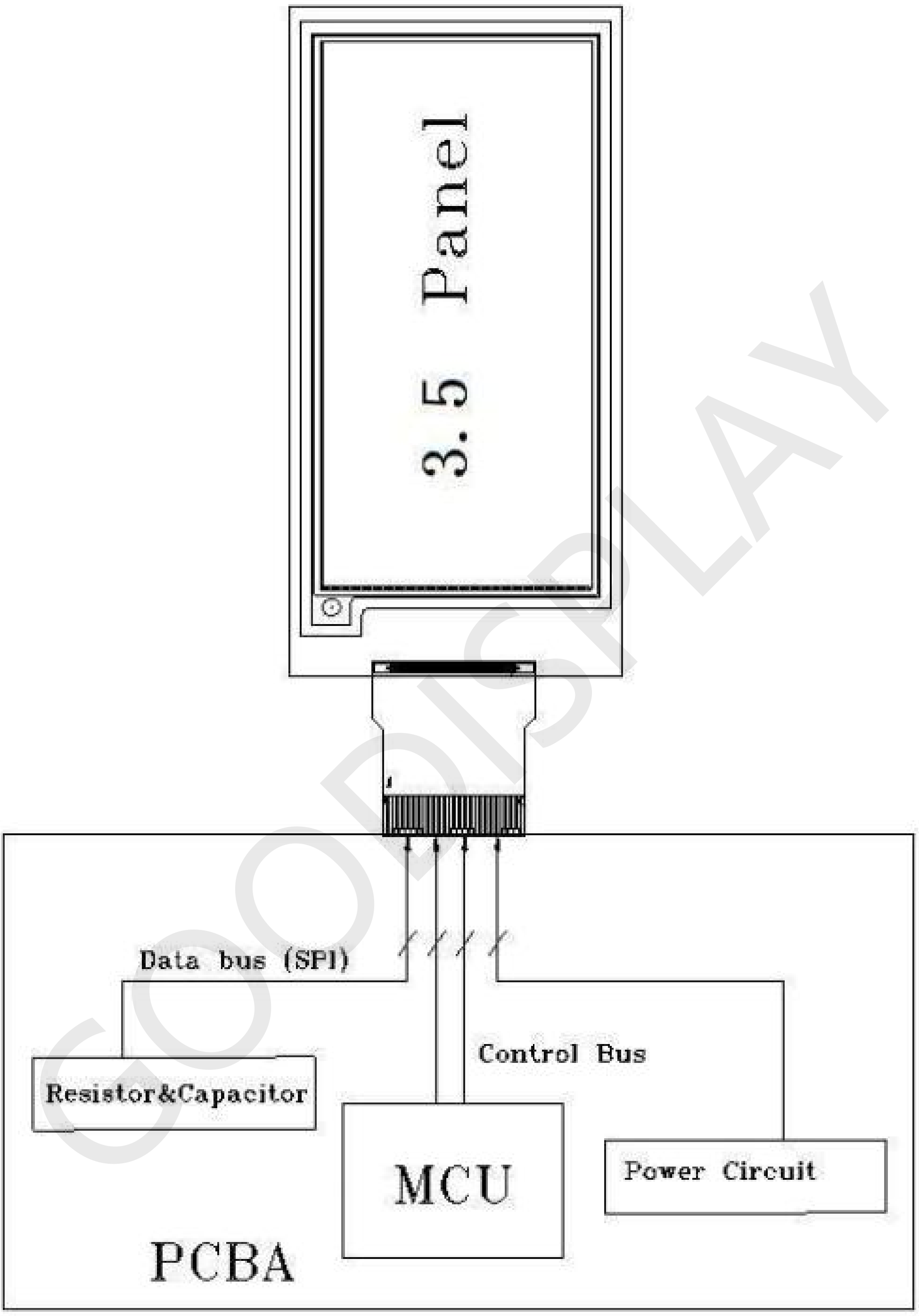
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display update sequence The Display update sequence option is located at R22h. Busy pad will output high during operation. user should not interrupt this operation to avoid corruption ofpanel images.
0	0	21	0	0	1	0	0	0	0	1	Display update control 1	RAM Content option for Display update A[7:0] - o0h [POR] B[7:0] - o0h [POR] A[7:4] Red RAM Option 0000 Normal 0100 Bypass RAM Content as 0 1000 Inverse RAM Content A[3:0] BWRAM Option 0000 Normal 0100 Bypass RAM Content as 0 1000 Inverse RAM Content B[7:6] Resolution select 00 Display resolution is 200x384 01 Display resolution is 184x384 10 Display resolution is 168x384 11 Display resolution is 216x384
0	1		A7	A6	A5	A4	A3	A2	A1	AO		
0	1		B7	B6	0	0	0	0	0	0		

<table>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display update control 2</td><td rowspan="2">Display update sequence option:
Enable the stage for MasterActivation
A[7:0] = FFh (POR)
<table>
<tr><td>operating scquence</td><td>parameter (in Hex)</td></tr>
<tr><td>Enable clock signal</td><td>80</td></tr>
<tr><td>Disable clock signal</td><td>01</td></tr>
<tr><td>Enable clock signal
EnableAnalog</td><td>Co</td></tr>
<tr><td>Disable Analog
Disable clock signal</td><td>03</td></tr>
<tr><td>Enable clock signal
Load LUT With DISPLAY Mode 1
Disable clock signal</td><td>91</td></tr>
<tr><td>Enable clock signal
Load LUT With
DISPLAY Mode 2
Disable clock signal</td><td>99</td></tr>
<tr><td>Enable clock signal
Load temperature value Load
LUT With DISPLAYMode 1
Disable clock signal</td><td>B1</td></tr>
<tr><td>Enable clock signal
Load temperature value
Load LUT With DISPLAYMode 2
Disable clock signal</td><td>B9</td></tr>
<tr><td>Enable clock signal
Enable Analog
Display with DISPLAY Mode 1
Disable Analog
Disable Osc</td><td>C7</td></tr>
<tr><td>Enable clock signal
Enable Analog
Display with DISPLAY Mode 2
Disable Analog
Disable Osc</td><td>CF</td></tr>
<tr><td>Enable clock signal
Enable Analog
Load temperature value
DISPLAY With DISPLAY Mode 1
Disable Analog
Disable Osc</td><td>F7</td></tr>
<tr><td>Enable clock signal Enable Analog
Load temperature value
DISPLAY With DISPLAY Mode 2
Disable Analog
Disable Osc</td><td>FF</td></tr>
</table></td></tr>
<tr><td></td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>AO</td></tr>
</table>

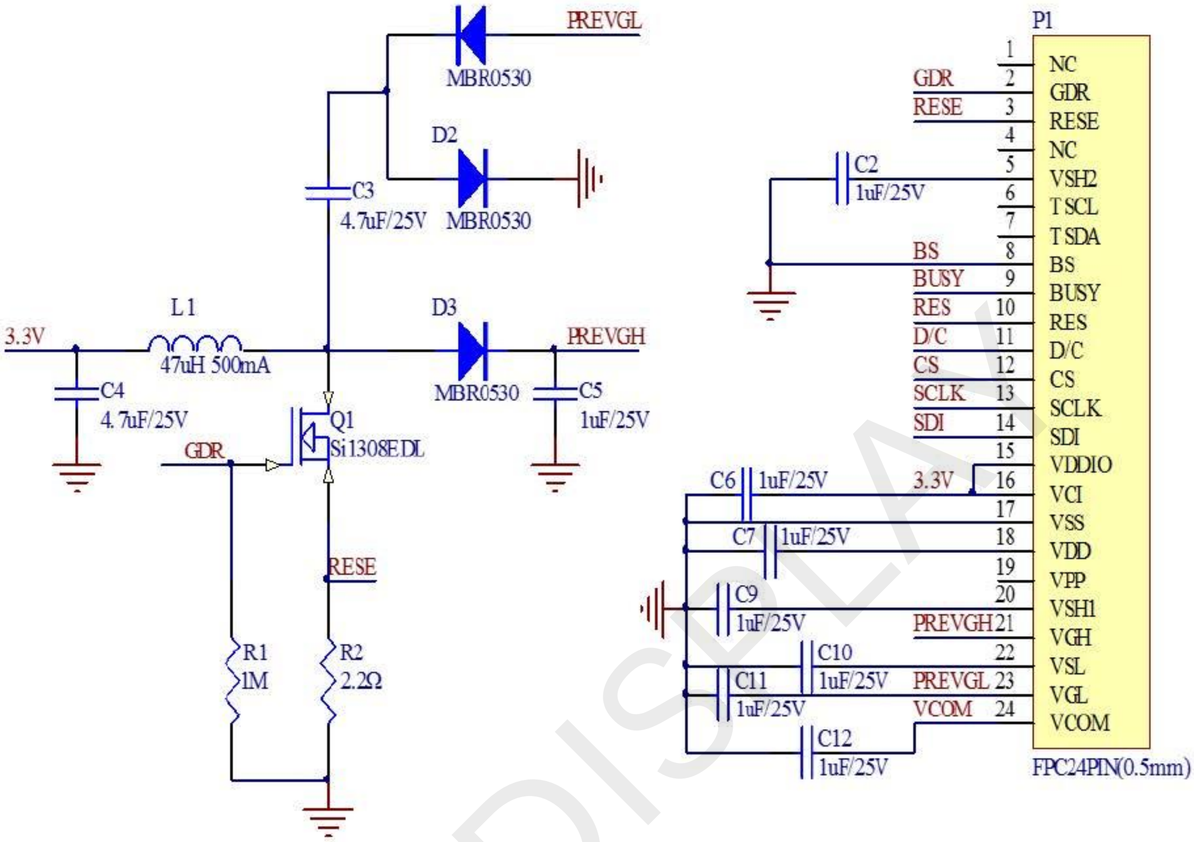
0	0	24	0	0	1	0	0	1	0	0	write RAM (Blackwhite) / RAM	After this command, data entries will be written into the BW RAM Until another command is written. Address pointers will advance accordingly. For write pixel: content ofwrite RAM(BW) = 1 For Black pixel: content ofwrite RAM(BW) - 0
0	0	26	0	0	1	0	0	1	1	0	write RAM (RED) / RAM	After this command, data entries will be written into the RED RAM Until another command is written. Address pointers will advance accordingly. For Red pixel: content ofwrite RAM(RED) = 1 For non-Red pixel [Black or white]: content ofwrite RAM(RED) = 0
0	0	2C	0	0	1	0	1	1	0	0	write VCOM register	set A[7:0]-4Bh
0	1		A7	A6	A5	A4	A3	A2	A1	AO		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display option	Read Register for Display option: A[7:0]: VCOM OTPselection (command ox37, ByteA) B[7:0]: VCOM Register (commandox2c) C[7:0]~G[7:0]: Display Mode (command ox37, Byte B to ByteF) [5 bytes] H[7:0] ~k[7:0]: waveform version (command ox37, Byte G to Byte J) [4bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	AO		
1	1		B7	B6	B5	B4	B3	B2	B1	BO		
1	1		C7	C6	C5	C4	C3	C2	C1	Co		
1	1		D7	D6	D5	D4	D3	D2	D1	DO		
1	1		E7	E6	E5	E4	E3	E2	E1	EO		
1	1		F7	F6	F5	F4	F3	F2	F1	FO		
1	1		G7	G6	G5	G4	G3	G2	G1	GO		
1	1		H7	H6	H5	H4	H3	H2	H1	HO		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	JO		
1	1		K7	K6	K5	K4	K3	K2	K1	Ko		
0	0	2F	0	0	1	0	1	1	1	1	status Bit Read	Read IC Status Bit [POROx01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1 : Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1 : VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1 : BUSY A[1 :0]: chip ID [POR=01] Remark: A[5] andA[4] status are not valid after RESET, they need to be initiated by command ox14 and command ox15 respectively.
1	1		0	0	A5	A4	0	0	A1	AO		

0	0	32	0	0	1	1	0	0	1	0	write LUT register	write LUT register from Mcu interface [227bytes] , which contains the content of VS[nx-LUTm] , TP[nx] , RP[n] , SR[nxy] , FR and xoN[nxy] Refer to session 6 .7 WAVEFORM SETTING
0	1		A7	A6	A5	A4	A3	A2	A1	AO		
0	1		B7	B6	B5	B4	B3	B2	B1	BO		
0	1		ı	ı	ı	ı	ı	ı	ı	:		
0	1		ı	ı	ı	ı	ı	ı	ı	:		
0	1		ı	ı	ı	ı	ı	ı	ı	:		
0	1		ı	ı	ı	ı	ı	ı	ı	:		
0	0	3C	0	0	1	1	1	1	0	0	Border waveform control	select border waveform for VBD A[7:0] = coh [POR] , set vBD as HIZ. A[7:6] :select vBD Option A[7:6] — select vBD as 00 — GS Transition, Defined in A[2] andA[1 :0] 01 — Fix Level Define A [5:4] 10 — VCOM 11[(POR] — HIZ A[5:4] Fix Level setting for VBD A[5:4] — VBD level 00 — VSS 01 — VSH1 10 — VSL 11 — VSH2 A[1:0] GS Transition setting for VBD VBD Level selection: o0b: VCOM ; 01b: VSH1; 10b: VSL; 11b: VSH2 A[1 :0] — VBD Transition 00 — LUTO 01 — LUT1 10 — LUT2 11 — LUT3
0	1		A7	A6	A5	A4	0	0	A1	AO		
0	0	44	0	1	0	0	0	1	0	0	set RAM X - address start / End position	specify the startlend positions ofthe window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0] , X Start, POR = o0h B[5:0]: XEA[5:0] , X End, POR = 18h
0	1		0	0	A5	A4	A3	A2	A1	AO		
0	1		0	0	B5	B4	B3	B2	B1	BO		
0	0	45	0	1	0	0	0	1	0	1	set Ramy-address start / End position	specify the start/end positions ofthe window address in they direction by an address unit for RAM A[8:0]: YSA[8:0] , y start, POR = 012Bh B[8:0]: YEA[8:0] , Y End, POR = o000h
0	1		A7	A6	A5	A4	A3	A2	A1	AO		
0	1		0	0	0	0	0	0	0	A8		
0	1		B7	B6	B5	B4	B3	B2	B1	BO		
0	1		0	0	0	0	0	0	0	B8		
0	0	4E	0	1	0	0	1	1	1	0	set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: XAD[4:0] , POR is o0h
0	1		0	0	0	A4	A3	A2	A1	Ao		
0	0	4F	0	1	0	0	1	1	1	1	set RAM Y address counter	Make initial settings for the RAMY address in the address counter (AC) A[8:0]: YAD[8:0] , POR is 012Bh
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		

8.Block Diagram



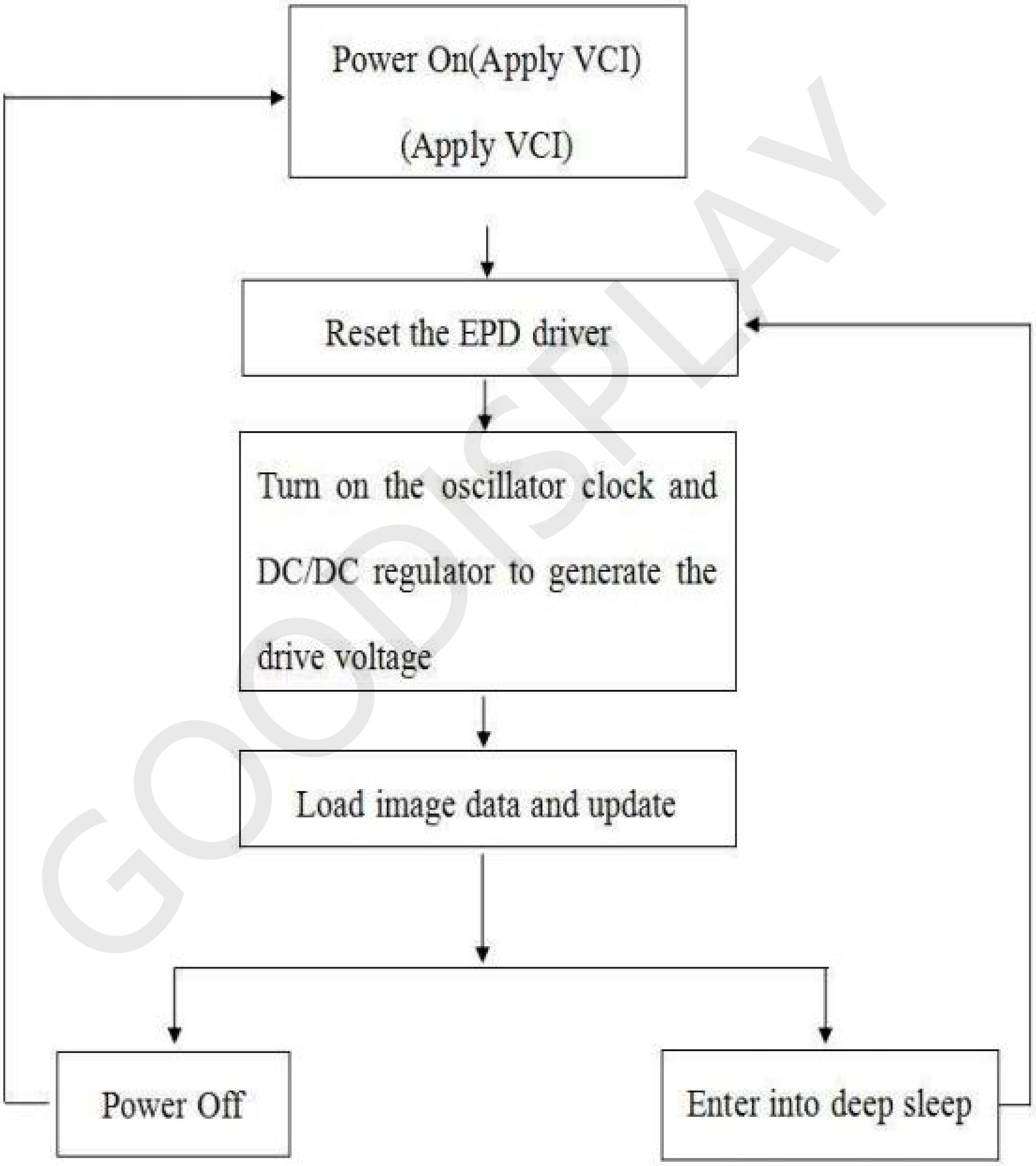
9 .Typical Application circuit with spI Interface



PartName	Requirementsforsparepart
C1—C12	0603/0805;X5R/X7R;VoltageRating:≥25V
R1、R2	0603/0805;1%variation,≥0.05W
D1—D3	MBR0530:1)ReverseDCVoltage≥30V2)Io≥500mA 3)Forwardvoltage≤430mV
Q1	Si1308EDL:1)Drain-Sourcebreakdownvoltage≥30V 2)Vgs(th)≤1.5V3)Rds(on)≤400mΩ
L1	refertoNR3015:Io=500mA(max)
P1	24pins,0.5mmpitch

10 .Typical Operating sequence

10 . 1 LUT from OTp operation Flow



10 .2 OTp operation Reference program code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RES#	low	Hardware reset
delay	200us	
RES#	high	
delay	200us	
Read busy pin		wait for busy low
command oxl2		software reset
Read busypin		wait for busy low
SET VOLTAGE AND LOAD LUT		
LOAD IMAGE AND UPDATE		
command ox24	7500bytes	Load image (200/8*300)(BW)
command ox20		
Read busy pin		wait for busy low
command oxlo	Data ox01	Enter deep sleep mode
POWER OFF		

11 . Reliability Test

NO	Test items	Test condition
1	Low-Temperature storage	T = -25oc, 240 h Test in white pattern
2	High-Temperature storage	T = +70ec, RH=40% ,240h Test in white pattern
3	High-Temperature operation	T = +50ec, RH = 30% ,240h
4	Low-Temperature operation	oc， 240h
5	High-Temperature, High-Humidity operation	T=+40C， RH=90%,240h
6	High Temperature, High Humidity storage	T=+60C， RH=80%,240h Test in white pattern
7	Temperature cycle	1 cycle:[-25ec 30min]→[+70 ec 30 min] ： 100 cycles Test in white pattern
8	ESD Gun	Air+/-4kv;contact+/-2kv contact+-2kv(HBM C: 100PF;R: 1 .5k ohm) contactt/-200v(MM C:200PF;R:0 ohm) (Naked EPD display,including IC and FPC area)
9	Uv exposure Resistance	762w/m2 for 168hrs,40ec Test in white pattern

Note: 1 . stay white pattern for storage and non-operation test.
2. operation is black→white pattern, the interval is 150s.

12. Quality Assurance

12.1 Environment

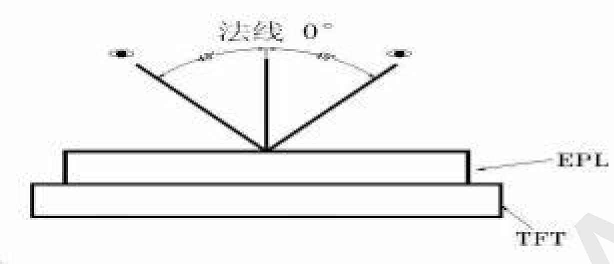
Temperature: 23±3℃

Humidity: 55±10%RH

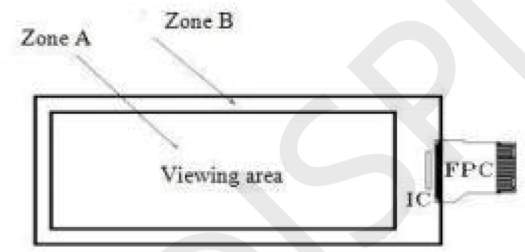
12.2 Illuminance

Brightness: 12001500LUX;distance:20-30CM;Angle:Relate 45osurround.

12.3 Inspect method

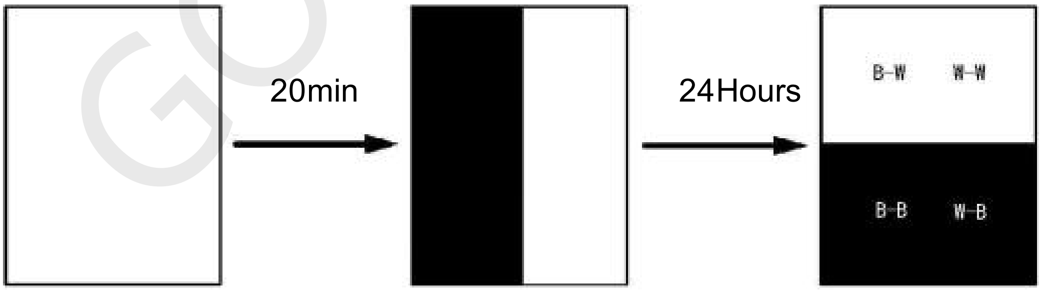


12.4 Display area



12.5 Ghosting test method

Two-color ghosting is measured with following transition from horizontal2 scale pattern to vertical 2 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by DKE.



1) Measurement Instruments: X-rite i1pro

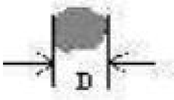
2) Ghosting formula:

w ghosting: $\triangle L = \mathrm{Max}\ (\Delta L(WW\text{-}W,\ B\text{-}W)) - \mathrm{Min}\ (\Delta L(W\text{-}WB\text{-}W))$

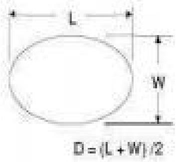
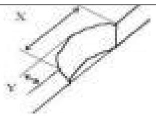
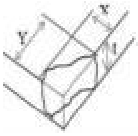
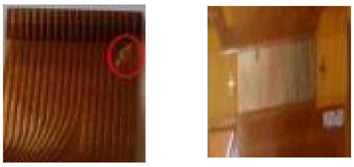
kghosting: $\triangle L = \mathrm{Max}\ (\Delta L(W\text{-}B,\ B\text{-}B)) - \mathrm{Min}(\Delta L(W\text{-}B,\ B\text{-}B))$

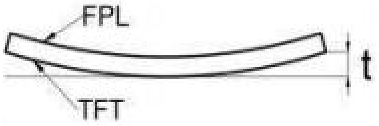
12.6 Inspection standard

12.6.1 Electric inspection standard

NO.	Item	standard	Defect level	Method	scope
1	Display	Display complete Display uniform	MA	visual inspection	zone A
2	Black/white spots	 D≤0.25mm, Allowed 0.25mm<D≤0.4mm. N≤4allowable D>0.4mm is not allowed	MI		
3	show B/w lines	 L≤0.4mm, w≤0.1mm negligible 0.4mm<L≤1.omm 0.1mm<w≤0.4mm N≤4 allowable L>1.omm, w>0.4mm is not allowed		visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	visual inspection	
5	Flash dot / Multilateral	Flashpoints are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	visual/ Inspection card	zone A zone B
6	segmented display	selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	visual inspection	zone A
7	shortcircuit/ circuit break/ Display abnormal	Not Allow			

12.6.2Appearance inspection standard

NO.	Item	standard	Defect level	Method	scope
1	B/W Spots /Bubble/ Foreign bodies/ Dents	 D≤0.25mm negligible 0.25mm<D≤0.4mm N≤4 allowable D>0.4mm is not allowed	MI	visual inspection	zone A
2	Glass crack	NotAllow	MA	visual / Microscope	zone A zone B
3	Dirty	Allowed if can be removed	MI		zone A zone B
4	chips/scratch/ Edge crown	 X≤3mm,y≤0.5mm And without affecting the electrode is permissible  2mm≤x or 2mm≤y Not Allow  W≤0.1mm,L≤5mm, No harm to the electrodes and N≤2 allow	MI	visual / Microscope	zone A zone B
5	TFT cracks	 Not Allow	MA	visual / Microscope	zone A zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	visual / Microscope	zone A/ zone B
7	Fpc broken/ Goldfingers xidation/ scratch	 NotAllow	MA	visual / Microscope	zone B

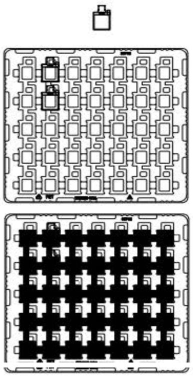
8	B/w Line	 L≤1 .omm,w≤0. 15mm negligible 1 .omm<L≤4.omm 0. 15mm<w≤0.5mm N≤4 allowable L>4 .omm ,w>0. 5mm is not allowed	MI	visual / Ruler	zone B
9	TFT edge bulge /TFT Chromatic aberration	TFT edge bulge : X≤3mm , Y≤0. 3mm Allowed TFT Chromatic aberration :Allowed	MI	visual / Microscope	zone A zone B
10	Electrostatic point	D≤0.25mm, allow 0.25mm<D≤0.4mm ,n≤4 allow D>0 .4mm is not allowed (n≤8 items are allowed within 5 mm in diameter)	MI	visual / Microscope	zone A
11	PCB damaged/ poor welding/ curl	PCB (circuit area) damaged Not Allow PCB poor welding Not Allow PCB Curl≤1%	MI	visual / Ruler	zone B
12	Edge glue height/ Edge glue bubble	Edge Adhesives H≤ps surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble: bubble width ≤1/2 Margin width; Length ≤0.5mmo n≤5			
13	protect film	surface scratch but not effect protect function, Allowed		visual Inspection	
14	silicon glue	Thickness≤ps surface(with protect film): Full cover the IC; shape: The width on the FPC ≤ 0.5mm (Front) The width on the FPC≤1 .omm (Back) smooth surface, No obvious raised.	MI	visual Inspection	
15	warp degree (TFT Substrate)	 t≤1 .omm	MI	Ruler	
16	color difference in COM area (silverpoint area)	Allowed		visual Inspection	

13.Packaging

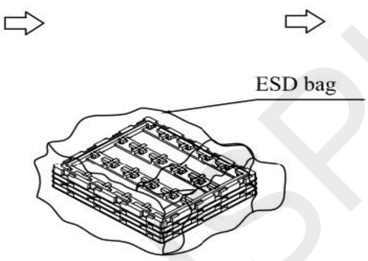
CUSTOMER'S APPROVED:		PAGE: 1/1

PACKLING ORDER:

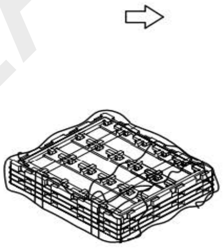
1) Putting 35 pcs Modules on each PET tray.And cover a dedicated EPE film.



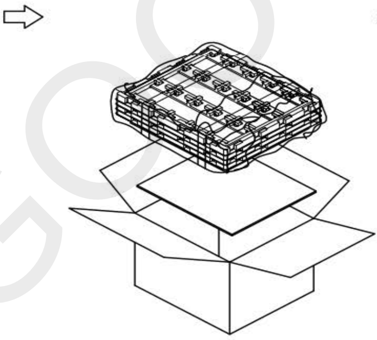
2) Putting 12 pcs PET trays together with 1 empty tray on the top of PET tray. Insert in the ESD bag, add desiccant in the ESD bag.



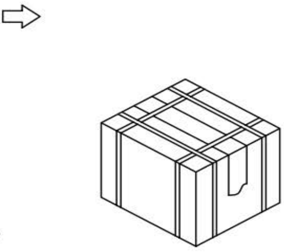
3) the tray together with adhesive tape



4) Putting into one outcarton



5) Packing finished



Note:35 pcs in a tray, 12 trays in a inner carton, 1 inner cartons in a out carton, so 35x12x1=420pcs/Outcarton

Dimension (Out carton): 394*344*255mm

	Drw:	Chk:	Apv:

14.Precautions

(1)Do not applypressure to the EPD panelin order to prevent damagingit.

(2)Donot connect or disconnect theinterfaceconnector whiletheEPDpanelisin operation.

(3)Do not touch IC bondingarea. It may scratch TFT lead or damage IC function.

(4)Please bemindful ofmoisture to avoiditspenetrationinto theEPD panel, which may cause damage duringoperation.

(5)High Temperature,high humidity, sunlight or fluorescent light may degrade the EPD panel ’ s performance. Please do not expose the unprotected PDpanel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.